# Cost Comparison of Fan-out Wafer Level Packaging and Flip Chip Packaging

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## Abstract

In recent years, there has been increased focus on fan-out wafer level packaging. While fan-out wafer level packaging may be the right solution for many designs, it is not always the lowest cost solution. The right packaging choice is the packaging technology that meets design requirements at the lowest cost. Flip chip packaging, a more mature technology, continues to be an alternative to fan-out wafer level packaging. It is important for many in the electronic packaging industry to be able to determine whether flip chip or fan-out wafer level packaging is the most cost-effective option.

This paper compares the cost of flip chip and fan-out wafer level packaging across a variety of designs. Additionally, the process flows for each technology are introduced and the cost drivers highlighted. Activity based cost modeling is used for this analysis. The goal of this cost comparison is to determine which design features drive a design to be packaged more cost-effectively as a flip chip package, and which design features result in a lower cost fan-out wafer level package.

## Key words

Cost comparison, Fan-out wafer level packaging, Flip chip, Yield

## I. Introduction

At the end of 2015, it was said that fan-out wafer level packaging was filling the gap between fan-in packaging and flip chip packaging [1]. Fan-in technology allows for a package that is thinner than flip chip technology, but the number of I/Os are limited because the die and package are the same size. Fan-out technology does not have the same I/O limitations.

With flip chip and fan-out technology both suitable from a technical perspective for many applications, it is important to understand the cost of each technology. The right package is the package that meets design requirements at the lowest cost. There have been many advancements in fan-out technology in recent years and more are expected, but flip chip packaging is a mature alternative that also continues to see improvements [3]. Both technologies will be discussed separately before a direct cost comparison is carried out.

## II. Process Flows

### *A. Flip Chip Packaging*

The flip chip process begins with the fabrication of a substrate, and then die with bumps or copper pillars are assembled onto the substrate. The key activities for a typical flip chip process are outlined in Fig. 1

Some process variations may exist. The yellow boxes indicate steps that occur on the incoming semiconductor wafer. After semiconductor processing, bumps or copper pillars must be added to the wafer before it can be diced and placed in the flip chip package. This diagram shows the die being attached and then underfill being applied, but a nonconductive film or paste may be used instead of underfill. Alternatively, a molded underfill may be applied instead. There also may be an overmold step in some flip chip processes. Key flip chip cost drivers are package size, substrate structure, and the cost of bumping the incoming wafer.

### *B. Fan-out Wafer Level Packaging*

There are a few varieties of fan-out wafer level packaging on the market right now. The version analyzed in this comparison is a die-first face-down process, outlined in Fig. 2.

Unlike the flip chip process introduced above, there are not separate substrate and assembly portions of the fan-out process. The incoming semiconductor wafer is diced but not

bumped, and the substrate is essentially formed around the die in the fan-out process. Another difference between fan-out and flip chip processing is that there are two opportunities to scrap the flip chip package—at the end of the substrate creation, and at the end of the assembly process—whereas the only opportunity for scrap in the fan-out process occurs at the end of the flow.

Key cost drivers in the fan-out wafer level packaging are package size, the number of imaging steps (directly dependent on the number of redistribution layers required), and yield.

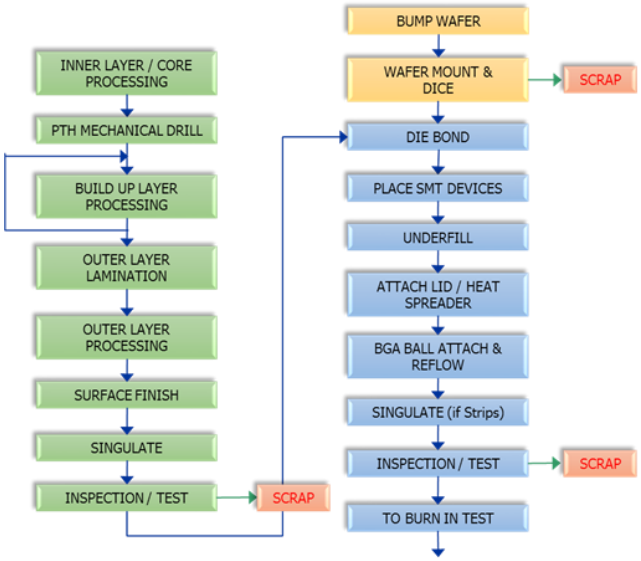


Figure 1. Flip Chip Process

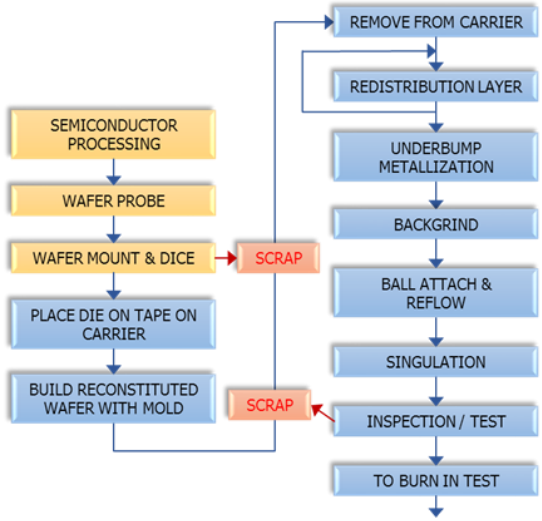


Figure 2. Fan-out Wafer Level Packaging Process

### C. *Yield Differences*

While there are many differences between the flip chip and wafer level packaging processes, as indicated in the flow charts above, there is one difference in particular that will have a notable impact on the cost comparisons in this analysis.

There are three points during the flip chip process flow when scrap may occur, but only two during the fan-out wafer level packaging process. In fan-out packaging, a wafer is brought in and diced; after dicing, bad die will be scrapped. The remaining good die are placed on the tape to begin the fan-out process, and all of the fan-out processing is completed before another scrap opportunity occurs. That means that any defects introduced during the packaging process will result in the loss of the die.

The same first scrap point occurs in flip chip packaging: a wafer is brought in, diced, bumped, and then bad die are scrapped. From there, the flip chip process diverges from the fan-out process. The fabrication of the flip chip substrate occurs next, the substrate can be tested after fabrication is complete, and there is an opportunity for scrap. This means that any defects introduced during substrate fabrication do not result in the loss of a die. Only assembly defects result in the loss of a die.

When comparing the cost of fan-out and flip chip packaging, the cost of processing is taken into account (including preparation of the incoming die), and the cost of any die scrapped must also be taken into account. The analysis that follows will first evaluate the cost of the processing costs alone, and then it will include the cost of the die and the cost of scrapping any die.

## III. Activity Based Cost Modeling

Activity based cost modeling was used to construct generic flip chip and die-first face-down fan-out wafer level packaging models. With activity based cost modeling, a process flow is divided into a series of activities, and the total cost of each activity is calculated. The cost of each activity is determined by analyzing the following attributes: time required, amount of labor required, cost of material required (consumable and permanent), tooling cost, all capital costs, and yield loss associated with the activity.

## IV. Cost Comparison

There are many factors that impact the cost of a design. Some of the most basic design details are the package size, die size, number of I/Os, and the substrate structure (in the case of flip chip packaging). To carry out a meaningful cost comparison between these two technologies, a variety of comparisons are carried out so that different variables can be isolated.

### A. *Varying Package Size*

The first set of data compares the cost of each package when packaging the same die in different package sizes. I/O count is driven by package size, so the I/O count is adjusted

accordingly as different package sizes are evaluated. Two die sizes are included in the analysis, and the flip chip design uses a 1-2-1 substrate. The charts below show the processing costs for both packaging types. Processing costs include the cost of processing, plus the cost of any processing that is scrapped. Neither the cost of the die, or the loss of any die, are included.

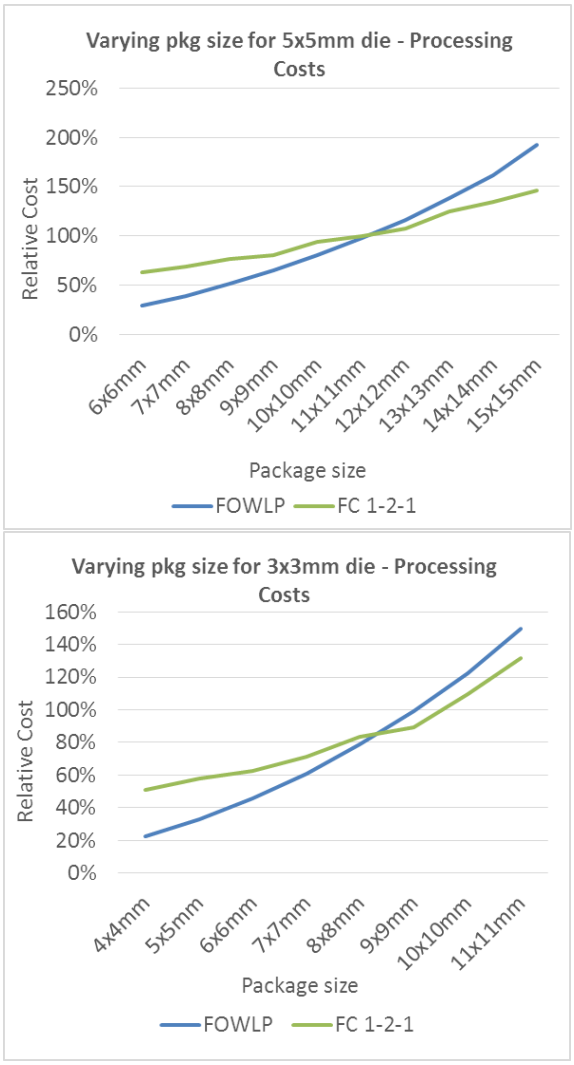


Figure 3. Varying Package Size

The first chart covers a range of package sizes for a 5x5mm die, while the second chart looks at a different range for a 3x3mm die. In the case of the larger die, the crossover point happens around the 11x11mm package point, which is when fan-out wafer level packaging stops being the more cost-efficient choice. With the smaller die, this crossover point happens earlier, around the 8x8mm package size.

The takeaway from both charts is that the larger the package size, the more likely flip chip processing will become cost-effective. However, the package size at which this occurs will depend on the design. The size of the package itself is less important than the size of the package in relation to the die. For fan-out processing, the smaller the package in relation to the die, the less mold required. This results in lower processing costs.

Flip chip packaging is not quite as sensitive to increasing package size. This is because flip chip packaging has a static die cost impacting the total cost; substrate and assembly costs changes with package size, but the die preparation cost does not change. On the other hand, having to include the cost of bumping the die as a flip chip processing cost is one reason flip chip packaging can be more expensive than fan-out wafer level packaging. The cost to bump a wafer is not insignificant.

### *B. Varying Die Size*

The next analysis keeps the package size constant while the size of the die being packaged changes. Similar to the previous example, all results are focusing on the cost of the processing only, not the cost of the die being packaged.

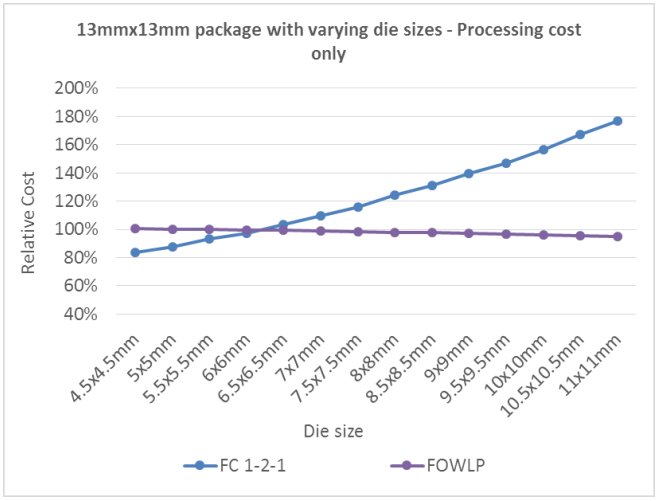


Figure 4. Varying Die Size – Processing Cost Only

The cost of the fan-out wafer level package is nearly static, with the cost actually going down at the larger die sizes, since larger die reduce the amount of mold required. On the other hand, the cost of the flip chip package changes with die size even though the package size is static, because a larger die brings in a higher processing (bumping) cost.

Next, the above example was repeated, but this time the cost of the die and scrapping of that die were taken into account. A one dollar and two dollar die were analyzed.

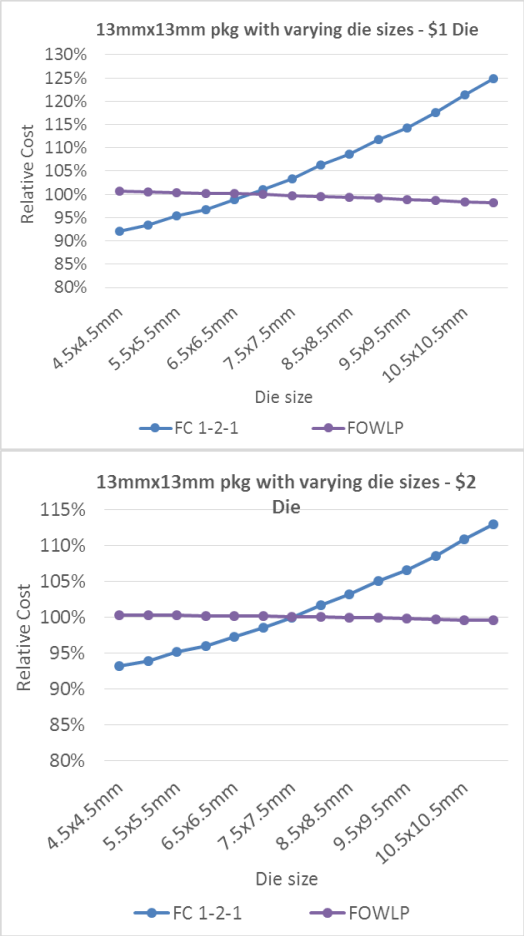


Figure 5. Varying Die Size – Die Cost Included

When only processing costs were taken into account, the crossover point was close to the 6x6mm die design. With a one dollar die, the crossover is pushed between the 6.5x6.5mm and 7x7mm die scenarios, and with a two dollar die, the crossover happens with a 7.5x7.5mm die. These graphs illustrate the fact that the more expensive the die being packaged, the higher the potential scrap cost of fan-out packaging. This increased scrap potential results in the flip chip designs being cost-effective for more scenarios as more expensive die are evaluated. This is due to the differing number of scrap points in the process flows, introduced earlier.

### *C. Yield Analysis*

In the second example above, the cost of the die was brought into the equation. It was shown that when taking only the cost of processing into account, fan-out wafer level packaging tends to be cost-effective for certain designs, but once the cost of the die and scrapping that die is included, flip chip packaging becomes advantageous in more cases.

Since the loss of die due to defects in the fan-out process is a key factor when comparing these two technologies, this section will analyze the impact of yield in more detail. The cost models use defect density assumptions for particular steps in the process flows to account for the introduction of defects. Defect density is the probability that a defect will occur in a $1cm^2$ area. The models assume that one defect anywhere within the package area will cause that package to be scrapped.

The following charts repeat the two previous examples—stable package size with changing die size, and stable die size with changing package size—but the defect density for the fan-out process is adjusted across a range. Two die costs are evaluated. The legend refers to the additional defect density added in each fan-out case. That 0.02 line corresponds with the baseline defect assumptions for a particular activity; the following lines account for an additional 0.02 defects per $1cm^2$ for one activity.

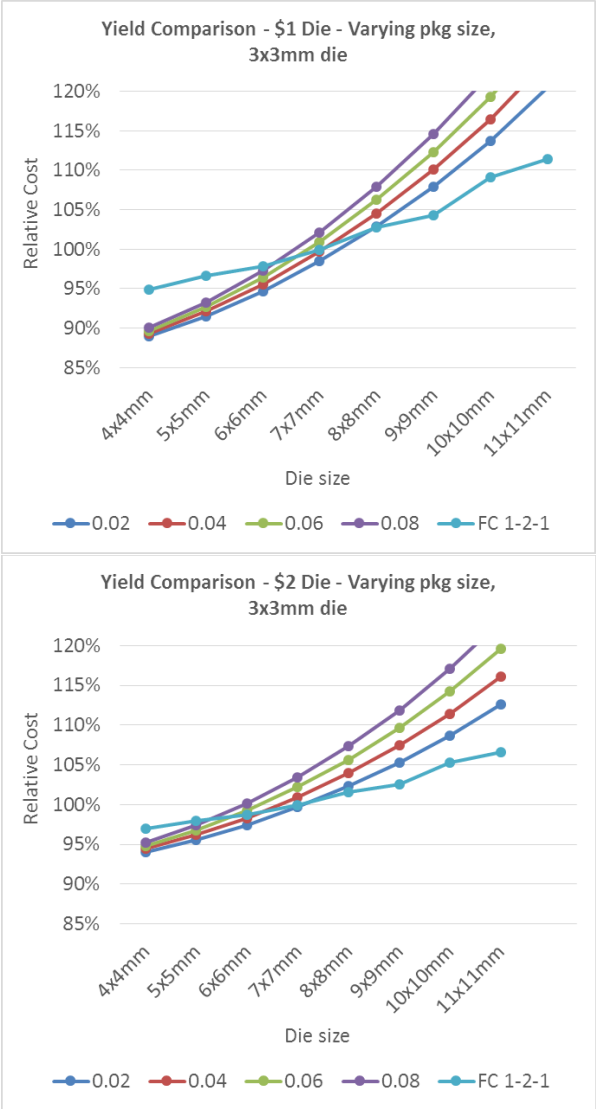


Figure 6. Varying Die Size – Yield Comparison

As a frame of reference, the defect density assumptions for the 7x7mm fan-out package equate to approximately a 1% yield loss with each color. Total yield for the 0.02 line is about 99%, total yield for the 0.04 line is about 98%, and so on. The yield for the flip chip process is also in the high nineties.

With the one dollar die example above, as the package size changes for the same 3x3mm die, the flip chip package is more expensive than the fan-out package with the best yield until the 8x8mm package mark. However, the flip chip package is about the same cost as the fan-out package with the lowest yield at a 6x6mm package. In the two dollar die example, the fan-out scenario with the best yield is more cost-effective than flip chip until a 7x7mm package, and the fan-out scenario with the worst yield is more cost-effective than flip chip only up to a 5x5mm package size.

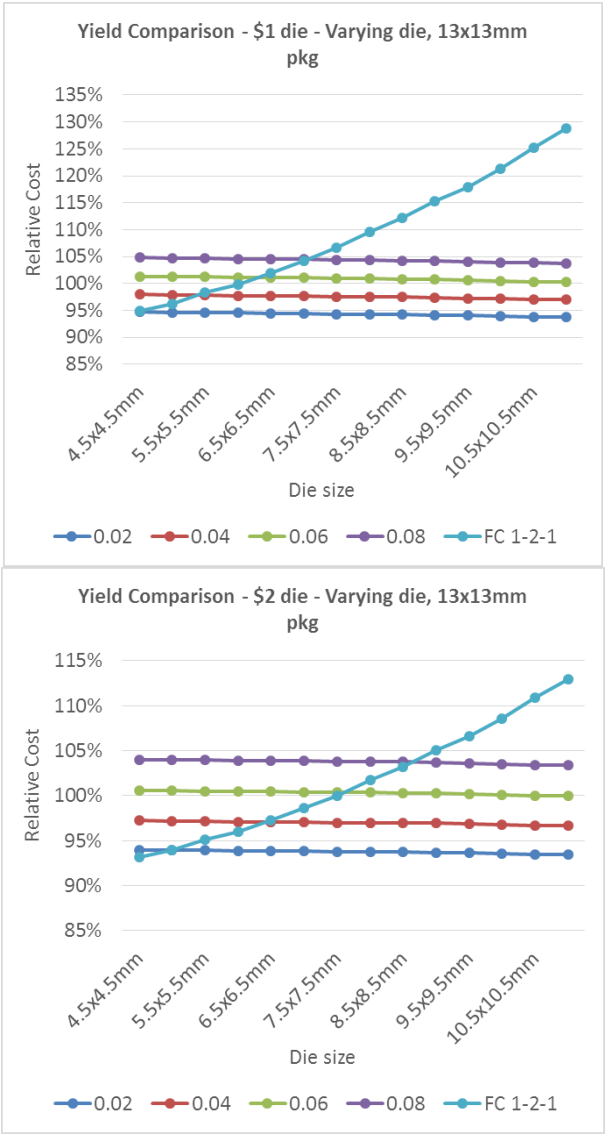


Figure 7. Varying Die Size – Yield Comparison

The above charts hold the package size at 13x13mm and vary the die size. When a one dollar die is taken into consideration, the highest yield fan-out package is cost-effective in nearly every scenario, having the same cost as the flip chip package for the smallest die size tested. The lowest yield fan-out package is only cost-effective beginning at a 7x7mm die size. For the two dollar die example, the highest yield fan-out package is cost-effective starting at a 5x5mm die, and the lowest yield fan-out package is more cost-effective than flip chip starting at a 9x9mm die.

## IV. Summary

The flip chip and fan-out wafer level packaging process flows were introduced and analyzed separately. The cost of flip chip packaging is sensitive to package size, substrate structure, and the cost of bumping the incoming wafer. Fan-out wafer level packaging cost is sensitive to package size, the number of redistribution layers, and yield. The two technologies were compared across a variety of designs, and different variables were held constant.

When analysis of the processing costs were carried out, one key takeaway was that flip chip packaging is more likely to be cost-effective at larger package sizes. The point at which it becomes cost-effective depends on the design details. On the other hand, the cost to bump the die that will be placed in a flip chip package is a primary reason that flip chip packaging can be more expensive than fan-out wafer level packaging.

The results shifted once the cost of the die and the cost to scrap that die were taken into account. Fan-out wafer level packaging has fewer scrap opportunities than flip chip packaging, which makes fan-out processing more sensitive to yield changes. Different defect density assumptions were made to illustrate how the crossover point between fan-out and flip chip packaging costs shift depending on the yield of the fan-out process. It was also shown that the more expensive the die being packaged, the more likely the flip chip package would be cost-effective.

## References


[1] M. Lapedus, “Fan-out Packaging Gains Steam,” Semiconductor Engineering, 2015.

[2] D. Butler, “Fan-Out Wafer Level Packaging: Breakthrough advantages and surmountable challenges,” Solid State Technology, 2016.

[3] J. Lau, “Recent Advances and New Trends in Flip Chip Technology”, Journal of Electronic Packaging, 2016.