

Cost Trade-off Analysis of PoP versus 3D TSV

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Abstract

Smart phones and tablets continue to show strong growth. IDC predicts that smart phone shipments will grow from 472 million units in 2011 to 982 million by the end of 2015. Shipments of tablets will exceed 50 million units in 2012. These products make use of the 3D package-on-package (PoP) configuration where the top package typically contains memory and the bottom package contains logic such as a processor. Increasingly, the logic device in the bottom package is using flip chip, including copper pillar. Almost 600 million PoPs were shipped in 2011 [1] and the infrastructure for this package is well established.

Performance requirements such as increased bandwidth and lower power are driving the adoption of 3D ICs designed with through silicon vias (TSVs). The timing for mass production in mobile applications depends on how the cost of the new technology compares with that of existing technologies.

Designers must understand the total cost of each alternative including the effect of die yield versus package yield to choose the lowest cost options. For example, it is not enough to only calculate the processing cost and yield of TSVs when considering a 3D solution. Designers must also calculate the cost of using a known good die (KGD) or “pretty good” die (PGD) versus a packaged IC and the yield effect of that die on the cost of the total package.

This paper provides an assessment of the total cost trade-offs between PoP and 3D TSV. The cost and yield for PoP fabrication, PoP assembly, die yield, TSV, and die stacking are included. A break even analysis is also provided to highlight the 3D TSV required costs and yields to achieve the same cost as a PoP solution. An update of technology and business issues that are considered barriers to 3D TSV adoption is included.

The Next Era: 3D Packaging

There are many approaches to 3D packaging. These include versions of system-in-package (SiP) such as stacked die, stacked packages— (PoP), package-in-package (PiP), and

chip-on-chip (CoC)—in production today as well as versions being discussed for the future such as system-on-package (SOP), 3D fan-out wafer level packages, and vertical side interconnection techniques. Applications for stacked die are typically portable products such as mobile phones, digital cameras, and music players but are also increasingly found in medical, industrial, and aerospace applications. The primary applications for PoP continue to be logic plus memory stacks for smart phones, but the technology is also popular in digital cameras, MP3 players, and other multimedia applications. One disadvantage of the PoP compared to the stacked die CSP is height. Substrate thickness and ball pitch/ diameter are key factors governing package height. There has been considerable work in both areas, resulting in lower profile packages. In addition some companies have developed new packages. For example, through molded via (TMV) is a new bottom PoP technology developed by Amkor. Package-in-package is an intermediate solution. It is similar to a stacked die package, except that one of the stacked devices is a memory package—essentially a very thin LGA—that is pre-tested before being assembled and molded into the package. The PiP is also similar to stacked die in that it offers a thin, standard package for board assembly, but it has lower risk than stacked die because the memory package is tested and is only used if it is good. PiP is found in portable products such as mobile phones and digital cameras [2].

While these packaging methods provide many benefits, the adoption of 3D through silicon via (TSV) technology offers the ultimate in 3D integration. TSV is the latest in a progression of technologies for stacking silicon devices in three dimensions (3D). Driven by the need for improved performance, methods to use short vertical interconnects to replace the long interconnects found in 2D structures have been developed. More than 50 research organizations are developing 3D TSV processes. Many companies have research activities in 3D TSV technology and numerous demonstration vehicles have been developed. Future applications for 3D TSV include memory such as DRAM, processors, and FPGAs. End products ranging from servers to mobile phones may eventually use 3D TSV packages. As

companies move from R&D into production, –the difficult work begins to address the issues of design, thermal management, test, and assembly [3].

The future success of 3D TSV packages depends on co-design. TechSearch International has recently conducted studies of a variety of industry participants to determine where the industry stands on adoption greater use of co-design practices. Designers and electronic design automation (EDA) vendors agree that the barriers to co-design are many. However, conversations with both groups reveal different perspectives on what the primary constraints are. Not surprisingly, package designers see the problem as the lack of appropriate tools, while EDA suppliers suggest that designers are reluctant to make the cultural changes necessary to take full advantage of co-design. On the user side, chip and package suppliers say that there are excellent point solutions for design of the chip, package and board, but they are not integrated. The lack of a common format among different EDA suppliers is a significant barrier. Even if an EDA vendor does offer a co-design tool or a data exchange format, neither can be used if the IDM uses one vendor's tool for package design and another vendor for IC design, which is typically the case. Additionally, the tools used by the IDM's customers for system and/or board design are different again. Improvements in co-design are critical for future systems [4].

Activity Based Cost Modeling

Activity based cost modeling and parametric cost modeling are the two dominant cost modeling methods. Parametric cost modeling is done by statistically analyzing a large number of actual results and creating a model to match those results. This backward looking “black box” approach is appropriate for modeling processes that change slowly over time or cannot be decomposed into individual activities.

On the other hand, activity based cost modeling is the most accurate cost modeling method for forward looking technology tradeoffs because individual activities are characterized and analyzed. The total cost of any manufacturing process is calculated by dividing the manufacturing process into a series of activities and totaling the cost of each activity. The cost of each activity is determined by analyzing the following attributes:

- The time required to complete the activity
- The amount of labor dedicated to the activity
- The cost of material required to perform that activity – both consumable and permanent material
- Any tooling cost
- The depreciation cost of the equipment required to perform the activity
- The yield loss associated with the activity

Activity based cost modeling is also well suited to comparing different technologies and manufacturing processes. The total cost of a product can be divided into the following three categories:

- Direct manufacturing cost
- Allocated factory overhead
- Profit margin

The direct manufacturing cost is easy to quantify and reasonably consistent across the industry. However, factory overhead and profit margin vary significantly between different manufacturing sites and companies. By using activity based cost modeling, the specific differences in manufacturing cost can be determined by comparing the direct manufacturing costs. This “relative” cost modeling makes it much easier to understand the cost impacts—good or bad—of design decisions and technology tradeoffs.

The graph in figure 1 shows a partial example of an activity based cost graph for many of the TSV fabrication process steps. Each activity contributes cost in one or more of the six categories shown. These categories are represented by the colored bars and the running total is the line on the graph. The activities shown in this graph represent the imaging of the silicon prior the deep reactive ion etch followed by copper plating to fill the TSVs. As expected, these activities include a significant amount of capital cost which is the purple bar.

Activity based cost modeling was used for this analysis and a complete activity based cost model was constructed for the PoP and TSV options.

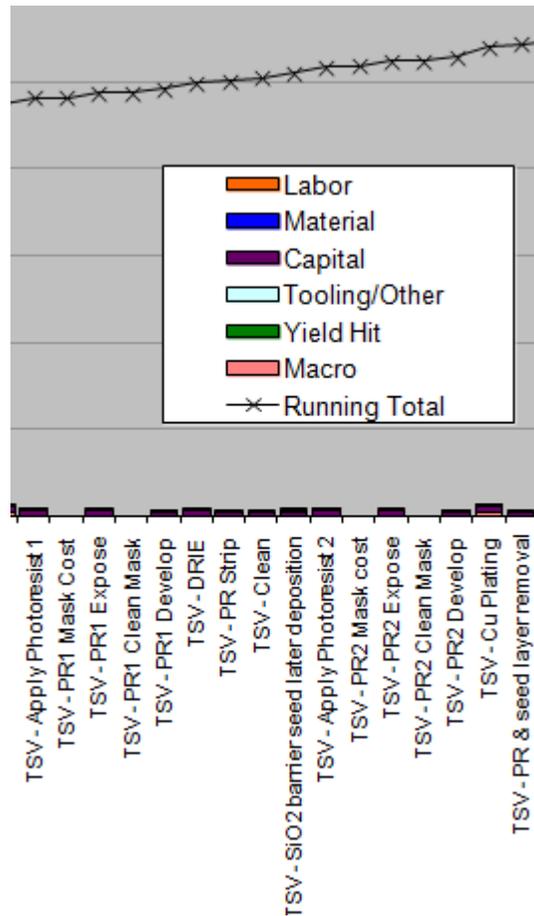


Figure 1 – Example of Activity Based Cost Modeling (Partial Cost Graph)

Baseline Results

We selected a typical mobile application case for a PoP compared to TSV cost comparison. The top die is a memory and the bottom die is a processor with the following dimensions –

- 14x14 mm package
- Top die is 10x10 mm with 200 connections to the bottom die
- Bottom die is 9.0x9.2 mm with 531 connections to the substrate

Figure 2 shows the two options considered in this comparison. The PoP option is implemented with through mold vias and the TSV option is implemented with a via middle process [5-11].

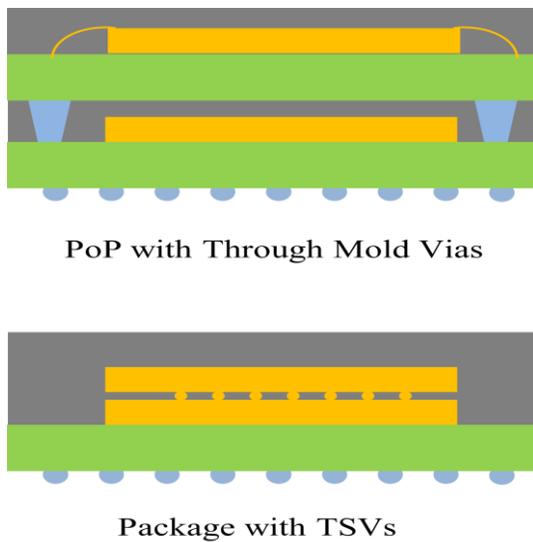


Figure 2 – TSV Versus PoP Implementation

Following are additional assumptions made for this comparison. Our goal is to make the two cases as similar as possible to isolate the cost differences and similarities associated with these two different approaches to stacking.

- For the PoP case, the bottom die is assembled using flip chip assembly and the top die is assembled using wire bonding.
- 2-2-2 structure used for the flip chip package
- 300 mm wafer for all die
- Wafer probe yield is 95% for all die
- Taiwan labor rates for everything
- All die are attached using nonconductive paste with no additional underfill
- TSVs are 10 micron in diameter and 50 microns deep
- Through mold vias are 400 microns wide and 400 microns deep.

- The bottom die in both cases is bumped using lead free solder bumping and the top die of the TSV case is micro bumped with copper.
- The yield loss of die after packaging is 1.5% for both the top and bottom die
- The yield per TSV is 99.96%
- In the TSV case, the area of the bottom die is not expanded to account for TSVs. We assumed there is enough area in the current 9.0x9.2 mm die to accommodate the TSVs (See section called “Effect of Growing the Bottom die to Accommodate TSVs” for more discussion of this assumption.)
- The only die costs included in this comparison are the wafer bumping and dicing costs. (See section called “Effect of Including Total Die Cost in the Analysis” for more discussion on die costs.)

Table 1 below shows the cost results for the PoP scenario

PoP Cost	Yield Loss	Cost
Bottom Package (including wafer bumping)		\$1.539
Top Package		\$0.999
Assembly		\$0.072
Bottom die - Yield Loss after packaging	1.50%	\$0.023
Top die - Yield loss after packaging	1.50%	\$0.015
TOTAL		\$2.648

Table 1 – PoP Cost Results

While both packages are 14x14 mm, the bottom package is more expensive because it includes through mold vias (TMVs) and is assembled using flip chip technology. The substrate for the bottom package also has an extra surface finish. The top package is a 14x14 mm wire bond package using gold wire. Assembly of the two packages is done during SMT pick and place using a solder paste dip process which is automated in most new SMT assembly equipment. There is not an extra reflow step because the top package and the bottom package can be reflowed at the same time. The die yield loss after packaging for each package does not compound since the packages are fully tested before they are stacked. Therefore yield loss on the top package only cause the top package to be scrapped and yield loss on the bottom package only causes the bottom package to be scrapped.

Table 2 below shows the cost results for the TSV scenario.

TSV Cost	Yield Loss	Cost
Bottom Package (including wafer bumping)		\$1.398
TSV Creation		\$0.331
Top Die Micro Bump and Place		\$0.597
Bottom die - Yield Loss after packaging	1.50%	
Top die - Yield loss after packaging	1.50%	
Yield Loss at Debond step	5.00%	
Yield Loss of 1 TSV (200 in package)	0.04%	
Cumulative Yield Loss	14.92%	\$0.408
TOTAL		\$2.734

Table 2 – TSV Cost Results

Unlike the PoP case, the die yield losses after packaging and the yield losses of the TSV manufacturing process compound. The only test and scrap opportunity other than wafer probe is at the end of the process and everything must be scrapped if the test fails. In addition to the TSV manufacturing yield loss, another source of defects results from thin wafer handling problems. This thin wafer handling yielded loss is typically introduced during the wafer debond step.

As shown in table 1 and table 2, the process cost for the TSV solution is less than the PoP solution. If zero yield loss is assumed for all steps, the process cost for PoP would be \$2.610 and the process cost for the TSV solution would be \$2.326. The extra cost of the PoP process is primarily due to the fact that there are two packages instead of one. However, if realistic yield loss is factored in to the comparison, the cost of a PoP solution is lower - \$2.648 for PoP and \$2.734 for TSV.

The next three sections show the cost sensitivity of varying key yield assumptions while keeping the other parameters constant at the values shown in table 1 and table 2.

Sensitivity Analysis of TSV Yield

One of the largest yield drivers is the yield per TSV. Given the large number of TSVs in 3D designs, the yield per TSV must be extremely high to make this solution cost effective. The chart in figure 3 shows a range of TSV yield from 99.8 percent up to 100%. Anything less than 99.8% will not be cost effective. A yield per TSV of 99.975% results in the same cost for the TSV and the PoP solution.

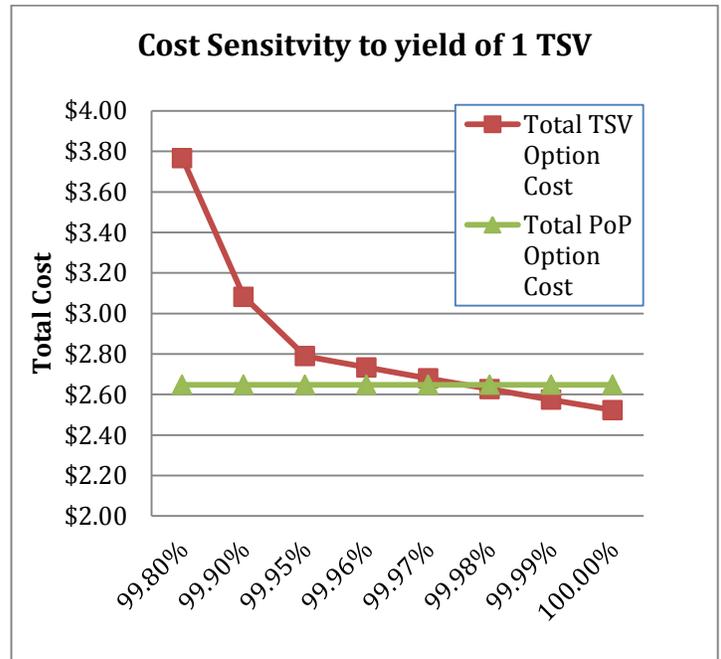


Figure 3 – TSV Yield Sensitivity

Another source of higher cost is yield loss due to thin wafer handling. This yield loss occurs during debonding of the temporary wafer after the wafer has been thinned to expose the TSVs. The graph in figure 4 shows the sensitivity of varying thin wafer handling yield. At 98% yield for thin wafer handling, the PoP option cost the same as the TSV option.

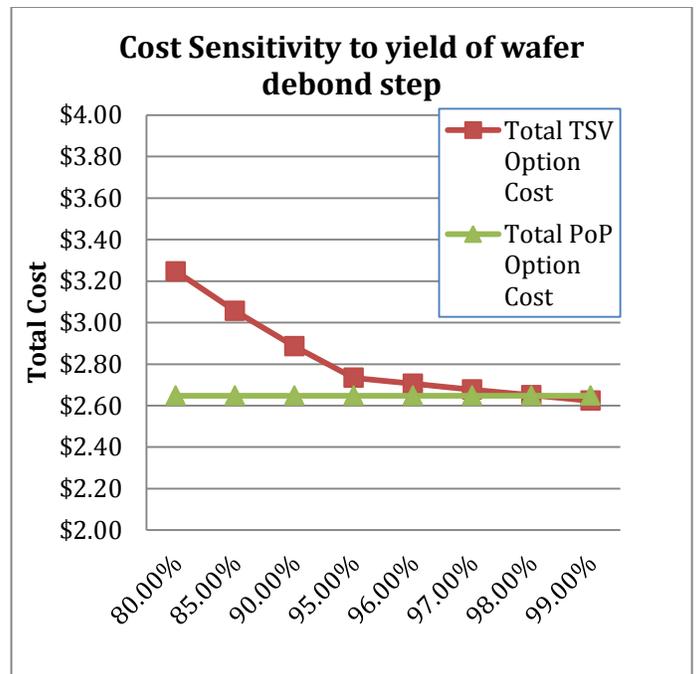


Figure 4 –Debonding Step Yield Sensitivity

Sensitivity Analysis of Yield Loss after Packaging

One of the major cost driver differences in PoP compared to TSV packages is the yield of the packaged die. This is all yield loss detected after die is packaged. It will include burn-in test yield loss, functional test of the package, and assembly defects. The reason the PoP scenario is less sensitive to this yield is because each of the two die are packaged and tested separately before stacking. Therefore, any failure in the top package only results in scrapping the top package and not the bottom package.

However, with the TSV scenario, both die are assembled in a single package. Therefore any failures during packaged die testing results in the scrapping of both the top and the bottom die. The graph in figure 5 shows that the die yield after packaging must be very close to 100% for the costs of the two options to be close. As with the other sensitivity analyses, all other variables are set at the baseline values in tables 1 and 2.

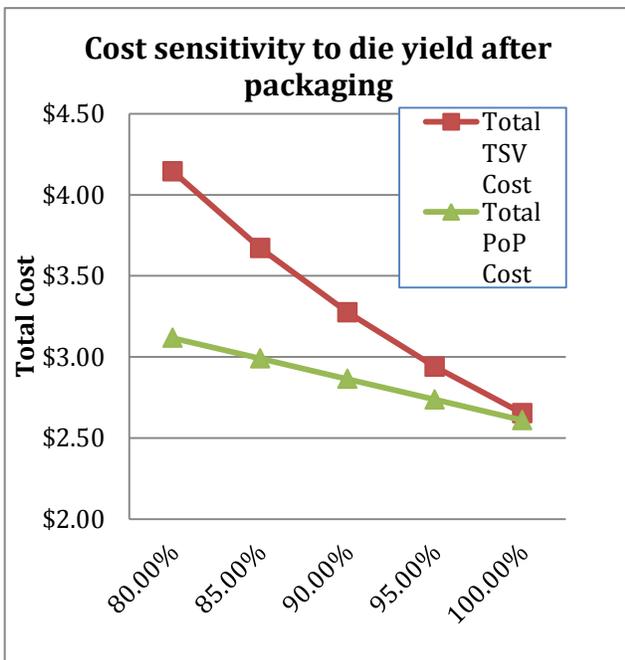


Figure 5 – Cost Sensitivity Due to Die Yield

Sensitivity Analysis of Number Top to Bottom Connections

Figure 6 shows a sensitivity chart of cost versus the number of top die to bottom die connections. In the PoP case, these will be done with TMVs and in the TSV case, they will be done with TSVs. The graph shows that the TSV option increases in cost more quickly than the PoP option. This is due to the compound effect of the TSV yield loss compared to the cumulative cost of TMV laser drilling. The graph goes all the way to 1000 connections for TSVs, but stops at 200 for TMVs. Given the size of the TMVs (400 microns in diameter) versus the size of the TSVs (10 microns in diameter), for a 14x14 mm package ~200 connections is the most that can be done without growing the size of the packages.

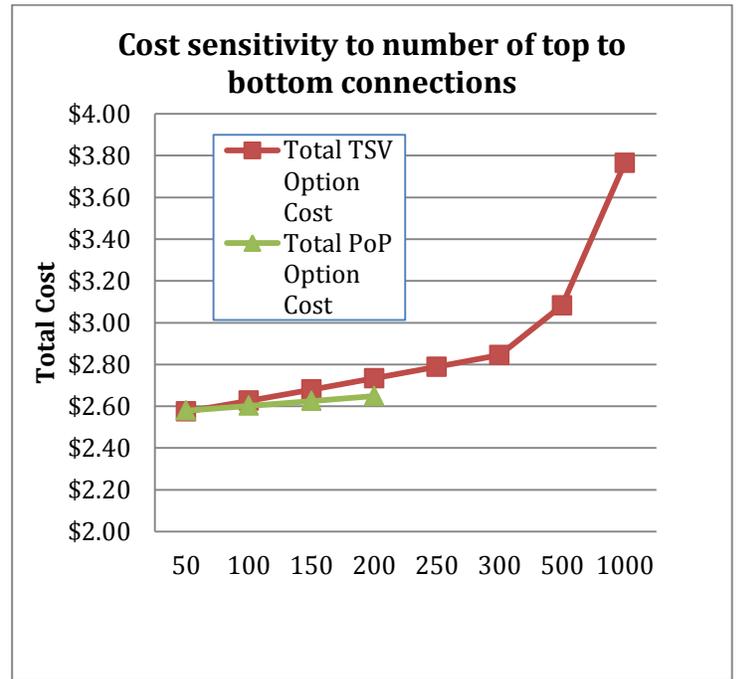


Figure 6 – Sensitivity to Number of Top to Bottom die Connections

Effect of Including Total Die Cost in the Analysis

Since the total cost of the silicon die will vary widely from application to application, this analysis focuses exclusively on the comparison of the packaging costs. However, given the different opportunities to test and scrap bad packages, die cost should be considered for specific comparisons.

The key yield numbers that will impact cost beyond the actual packaging costs are die yield loss after packaging of either die that is not detected during wafer probe plus yield loss resulting from defective TSVs and thin wafer handling. Die that fail during wafer probe are rejected before any packaging is done. Therefore, the wafer probe yield only has a small impact on the cost difference between the two approaches. However, any yield loss after the die is packaged will have a smaller effect on cost in the PoP case since only the top or the bottom packaged will be scrapped. In the TSV case, any packaged die yield loss from either die will cause both die and the package to be scrapped. Any yield loss from TSVs will cause all die and the package to be scrapped.

If the die are expensive, even a relatively small yield loss due to either the TSVs or yield loss after packaging will have a significant impact on cost. For example, if the total cost of the two silicon die is \$20.00, a 2% yield loss will add an extra \$0.40 to the TSV case but only \$0.20 to the PoP case.

Effect of Growing the Bottom die to Accommodate TSVs

One of the cost adders that may impact this comparison is the potential necessity to expand the bottom die in the TSV case. In addition to the 10-micron area for the TSV, there is an additional “keep out” area around the TSV. This area varies by fabricator but if we assume twice the via size, each TSV will consume 900 square microns of silicon area. Using these assumptions on the baseline case of 200 TSVs in a 9.0x9.2 mm die, the TSV area is only 0.022% of the total die area.

Even though this is a small percentage of the overall die area, it is possible that the required via locations may increase the size of the die. If the die is increased from 9.2x9.0 mm to 9.3x9.0, the cost increase of the TSV solution will be \$0.005.

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Conclusions

Following are the major conclusions from this analysis.

- Both packaged die yield and the TSV processing yield must be quite high for the TSV option to be cost effective. The baseline case of only 1.5% packaged die yield loss, 5% wafer handling loss, and .04% per TSV loss is still more expensive than the PoP case, but close. If any of these yield is significantly lower, the TSV case will become extremely expensive.
- With all other baseline parameter held constant, the per TSV yield for cost parity is 99.975%
- With all other baseline parameters held constant, the thin wafer handling yield for cost parity is 98%
- Given the size difference of the TSVs compared to the PoP through mold vias, PoP is not a feasible solution if a large number of top die to bottom die connections are required.

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