# COST COMPARISON OF MULTI-DIE FAN-OUT WAFER LEVEL PACKAGING AND 2.5D PACKAGING WITH A SILICON INTERPOSER

Chet Palesko, Amy Palesko
SavanSys Solutions LLC
10409 Peonia Ct
Austin, TX, 78733, USA
Ph: 512-402-9943
chetp@savansys.com, amyp@savansys.com

E. Jan Vardaman
TechSearch International, Inc.
4801 Spicewood Springs Road Suite 150
Austin, TX, 78759, USA
Ph: 512-402-9943 Email:
jan@techsearch.com

**ABSTRACT**
Miniaturization and performance requirements are driving product designers to use advanced packaging technologies. In many cases, these technologies are significantly more expensive than traditional packaging, but are necessary to meet the product requirements. Both fan-out wafer level packaging and 2.5D packaging on a silicon interposer enable designers to package multiple die in close proximity. This close proximity helps achieve miniaturization and may enable better performance since die to die interconnect is shorter.

In this paper we will compare and contrast the packaging cost drivers for multi-die fan-out wafer level packaging and 2.5D packaging on a silicon interposer. Total cost and yield plus individual activity cost and yield will be presented across a range of design characteristics including package size, die size, number of die, and number of IOs.

Key words: 2.5D, 3D, TSV, FOWLP, Cost, Interposer

**INTRODUCTION**
The best packaging choice is the one that meets the product requirements with the lowest cost. The two packaging technologies examined in this paper—fan-out wafer level packaging (FOWLP) and 2.5D packaging with a silicon interposer—are both expensive options compared to traditional packaging. However, in many cases the product requirements for performance, size, or IO bandwidth cannot be met using traditional packaging methods, and a designer must choose an advanced packaging alternative.

**FOWLP OVERVIEW**
FOWLP is a packaging technology that has characteristics of both traditional packaging and wafer level packaging (WLP). WLP adds processing necessary to mount and connect the active die to a printed circuit board. This processing is done while the silicon is still in wafer form and usually includes adding one or more redistribution layers (RDLs) and solder balls. This fabrication of the packaging technology directly on the wafer is in contrast to traditional packaging where the wafer is diced first and the die is placed on a substrate that has already been fabricated and tested. FOWLP technology applies the same wafer level redistribution layers and solder ball attach approaches as WLP, but these are applied to a re-constituted wafer instead of a silicon wafer. This re-constituted wafer has good die "islands" surrounded by mold.

The steps below describe the process flow for FOWLP as well as key cost and yield drivers.

- Dice probed wafers and discard the bad die. Scrapping bad die at this point in the process is an important cost avoidance step. Any bad die that are packaged will result in the scrapping of the bad die, the package, and any other die in the package.
- Place good die on a round temporary carrier that is either 200mm or 300mm in diameter. Final package size will be determined when the re-constituted wafer is diced, so more than one die can be placed in a single package. Accuracy of placement is critical for maintaining good yield.
- Build a re-constituted wafer using compression mold over and in-between the good die. Keeping the die stationary during this step is critical. Any movement of the die will result in yield loss because the connection to the die pads will fail.
- Add RDLs to the re-constituted wafer to distribute the package IOs as needed. Assuming the die have not moved, this activity has high yield but caries a moderate cost since an RDL involves multiple imaging steps
- Add solder balls to the reconstituted wafer. This is a high yield activity that is relatively low cost.
- Dice the re-constituted wafer into individual packages.

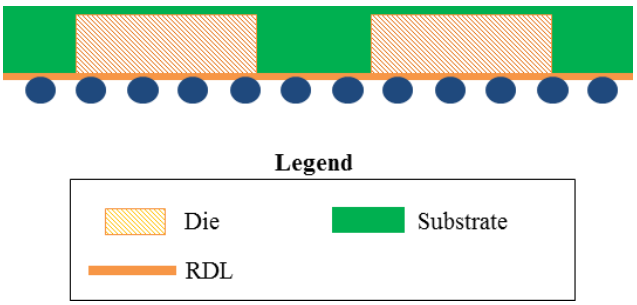


**Figure 1.** FOWLP Cross-section

## 2.5D OVERVIEW

2.5D technology has some of the benefits of full 3D vertical interconnect between two pieces of active silicon without the associated high costs and low yields. Both technologies rely on through silicon vias (TSVs) to form an electrical connection between the front and the back of a silicon wafer. Since TSVs are added at the wafer level, any yield loss resulting from the TSVs and associated interconnect process or from the fabrication of the active silicon will cause everything to be scrapped. With 3D technology, the TSVs are added directly to active silicon; this means potentially good active silicon is scrapped if there are defects in the TSVs. With 2.5D technology, TSVs and their associated interconnect are fabricated into an interposer (usually silicon) instead of directly into the active silicon. This allows the interposer and the silicon to be independently tested and scrapped before assembly into the final package.

The steps below describe the process flow for 2.5D packaging as well as key cost and yield characteristics.

*Fabrication of the Interposer*

- Start with an unprocessed silicon wafer and create TSVs by using a deep reactive ion etch (DRIE) process to form a deep hole partway through wafer. Then add oxide isolation and Cu plating to fill the hole. This TSV creation step must be done carefully because this is the electrical connection between the top and bottom of the silicon. The sidewalls of the TSVs must be smooth, and the Cu plating must be uniform. Given the required accuracy and importance of this activity, it is a significant cost and yield driver.
- Planarize the wafer using chemical mechanical planarization. This is a typical semiconductor CMP process.
- Add one or more RDLs to the top of the silicon interposer. The active die will be placed on this side, and the RDLs are necessary to connect the die pads to the tops of the TSVs.
- Temporarily bond the silicon interposer to a carrier wafer. This is a slow throughput step with a high cost because it is done one wafer at a time.
- Thin and planarize the interposer to reveal the bottom of the TSVs. This is a normal semiconductor process step.
- Debond the interposer from the temporary wafer. Since debonding is faster than temporary bonding, the process cost of this step is relatively low. However, after debonding from the rigid carrier wafer, the interposer is quite thin and there is a significant risk of thin wafer handling yield loss.
- Test and dice the interposer wafer and discard the bad interposers. Scrapping bad interposers at this point in the process is an important cost avoidance step. Any bad interposers that are assembled and tested will result in scrapping everything—interposer, active die, and substrate.

*Assembly and Final Packaging*

- Bump and dice the active silicon wafers. This is a high yield step, but relatively expensive and not required for FOWLP.
- Place the active die on the interposer using thermocompression bonding or solder plus reflow. Thermocompression bonding is slow and expensive, but if it is done in conjunction with non-conductive paste or film, underfill may not be necessary.
- Underfill the active die. This is optional, and total cost will be reduced if this step is avoided.
- Place the assembled silicon interposer on a substrate and overmold.
- Attach solder balls to the bottom of the substrate.

One factor not taken into consideration in the steps listed above is the method for temporary bond and debond of the carrier wafer. There is not yet one accepted, best practice for thin wafer handling in the industry. Therefore, depending on the method selected, factors like equipment and material cost, throughput, and yield may vary. The assumptions for the debond step in this paper only take into account the yield implications of thin wafer handling, not yield factors based on the particular debond method. For example, yield may be affected by residue remaining after debond, mechanical stress, or another factor unique to the bonding method used.

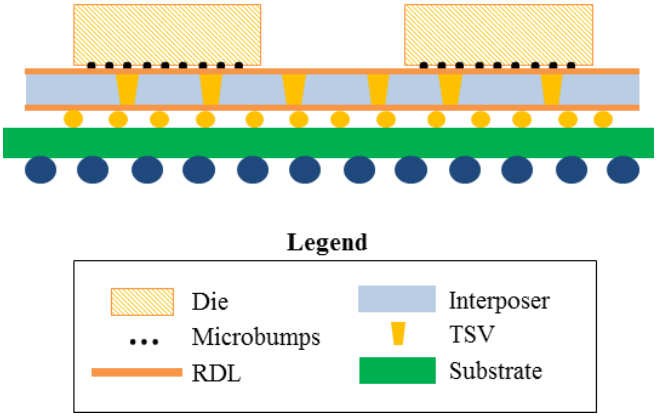


**Figure 2.** 2.5D Cross-section

## COST COMPARISON EXAMPLE

The example described below is a case of 3 medium sized (8mmx8mm) die placed in a single package. We chose this case to compare packaging using multi-die FOWLP and a 2.5D silicon interposer. This example would be difficult to package using traditional technology and still achieve close die proximity (high performance) and a high number of die to die IO connections.

The cost modeling for each of these cases was done using an activity based approach. In activity based cost modeling, the total cost of any manufacturing process is calculated by dividing the manufacturing process into a series of activities and totaling the cost of each activity. The cost of each activity is determined by analyzing the following attributes:

- The time required to complete the activity
- The amount of labor dedicated to the activity
- The cost of material required to perform that activity, both consumable and permanent
- Any tooling cost
- The depreciation cost of the equipment required to perform the activity
- The yield loss associated with the activity

An example of activity based costing results are shown in the graph in Figure 3. Each activity has the following cost components:

- Direct Labor—Determined by the time required to perform the activity times the percentage of an operator for that activity.
- Material—Both consumable and permanent material costs are included.
- Capital—This is calculated by allocating the equipment depreciation cost based on how long the product uses that equipment.
- Tooling cost—This will be any non-recurring engineering or fixtures.
- Yield hit—For assembly steps, this will be defects per million opportunities; for fabrication steps, this will be defects per square centimeter. Even though these defects are not visible until later in the process when testing is done, they add cost when they are created.

The graph shows the costs for the first series of activities for FOWLP. The two largest cost activities for this part of the manufacturing process are die bonding and compression molding. The die bond activity is expensive due to the equipment expense and relatively slow throughout. The material cost for the mold and post mold cure is also expensive.

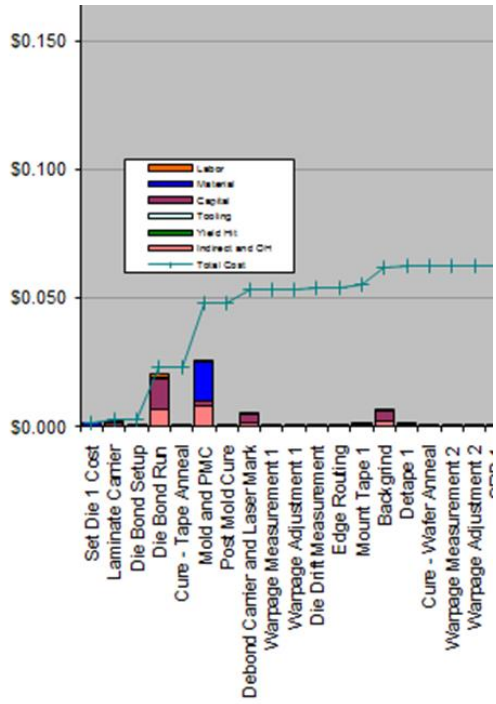


**Figure 3.** Activity Based Cost Results for FOWLP Initial Process Steps

The assumptions used for this cost comparison example are listed in Table 1 below.

**Table 1.** Technology Comparison Assumptions

| **Technology Comparison Assumptions** | |
|---|---|
| Package size | 20mmx20mm |
| Number of die | 3 |
| Cost of each die | $3.00 |
| Yield of each die (after wafer probe) | 100% |
| Die size | 8mmx8mm |
| Number of RDLs | 3 |
| Package IOs | 600 |
| Die to die connections | 1000 |
| Interposer fabrication yield | 90% |
| 2.5D die placement yield | 98% |
| FOWLP fabrication yield | 50% |
| FOWLP die placement yield | 98% |

The results of this example are shown in Table 2.

**Table 2.** Technology Cost Comparison Results

| FOWLP Vs. 2.5D Cost Comparison | | |
|---|---|---|
| | **2.5D** | **FOWLP** |
| Die Cost | $9.25 | $9.02 |
| Interposer Cost | $10.01 | |
| Interposer Scrap Cost | $1.00 | |
| FOWLP Fabrication cost | | $3.21 |
| FOWLP Fabrication Scrap Cost | | $1.29 |
| Die Placement Cost | $0.68 | $0.11 |
| Die Placement Scrap Cost | $1.50 | $0.83 |
| Substrate / Final Assembly Cost | $4.03 | $0.54 |
| **TOTAL** | **$26.47** | **$15.01** |
| *Scrap as % of total cost* | *9%* | *14%* |

The cost of the 2.5D packaging case is significantly more expensive than FOWLP. The main reason for this higher cost is the addition of an expensive interposer. As shown above, the interposer adds $11 to the 2.5D case, compared to nothing for the FOWLP case.

However, the design rule capabilities of the 2.5D technology are much finer than with FOWLP, so there are situations where FOWLP cannot be used and only a 2.5D solution (or putting everything on one die) will meet the product requirements. In general, FOWLP can be built with lines and spaces down to 10 microns. This is in contrast to 1 micron line and spacing for 2.5D designs. This difference in capabilities of one order of magnitude highlights the importance of pitch when considering FOWLP and 2.5D as packaging methods.

There is also a difference in the die preparation cost. 2.5D technology requires wafer bumping and FOWLP does not. Die placement is slightly more expensive in 2.5D technology given the fine pitch and thermocompression bonding, and 2.5D with an interposer still requires a substrate. In FOWLP, there is no substrate necessary since the package is fabricated around the die.

## YIELD SENSITIVITY

As discussed previously, yield is an important cost driver, and for this example we assumed the same activity yields for both cases. However, the 2.5D technology has an advantage by isolating the interposer yield loss and substrate yield loss by testing and scrapping each separately prior to final packaging. As with any packaging technology, die placement yield loss will result in scrapping everything.

FOWLP does not have the same isolation of yield loss advantage as 2.5D. Since the package is fabricated around the active die, any yield loss during fabrication will also result in scrapping of the die. This is demonstrated in the case above by comparing the scrap as a percentage of total cost. Even with the same activity yields, scrap is 14% of the total FOWLP cost and only 9% of the total 2.5D costs.

The graph in Figure 4 shows the scrap cost as a percentage of total cost for varying fabrication yields. For the 2.5D, the interposer fabrication yield is varied; for FOWLP, the yield of the re-constituted wafer process is varied. When the fabrication yields are 100%, the percentage of scrap for both technologies is the same. The only die scrapped will be due to defects in the assembly process. Since we are assuming the same assembly yield for both technologies, the scrap percentage will be the same.

However, as fabrication yields drop, a higher percentage of total cost is due to scrap with FOWLP packaging as compared to 2.5D packaging. This is because an increasing amount of die will be scrapped during the fabrication of the re-constituted wafer. In addition to low fabrication yields increasing FOWLP scrap costs, packaging more expensive die will have the same effect. Scrap costs can be high by scrapping a large percentage (low fabrication yield) of inexpensive die or by scrapping a small percentage (high fabrication yield) of expensive die. In either case, the FOWLP technology will cause die to be scrapped during fabrication, while 2.5D technology limits the die scrapping to assembly defects.

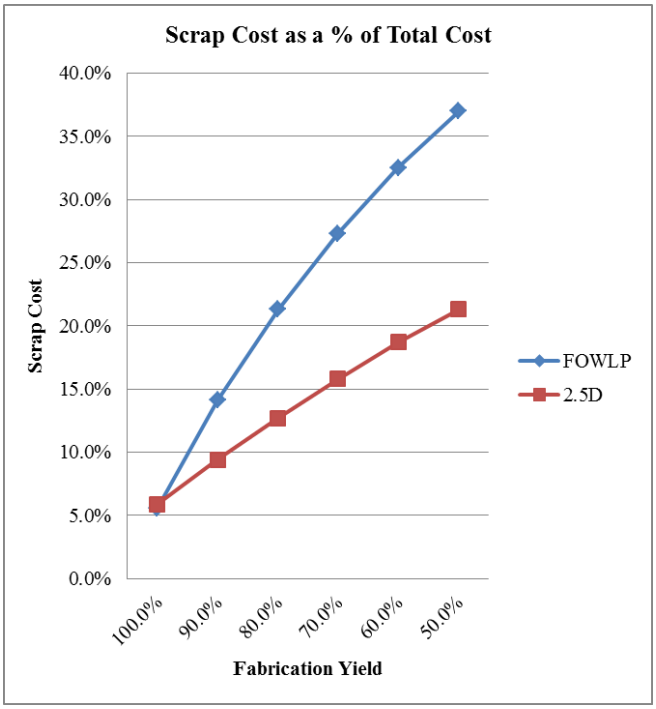


**Figure 4. Scrap Cost as a % of Total Cost**

**SUMMARY**

Following are the two key findings from this analysis.

- For multi-die packaging, FOWLP currently has a significant cost advantage compared to 2.5D technology using a silicon interposer. However, the 2.5D design rules are much finer than with FOWLP, so there may be cases where FOWLP will not be a good enough option to meet product requirements. However, if both technologies can be used to meet the product requirements, FOWLP will be more cost effective.
- The cost of FOWLP is more sensitive to low fabrication yields than 2.5D. While 2.5D packaging is more expensive, both the interposer and the substrate can be fabricated and tested before placing good die. This means good die will not be scrapped based on fabrication defects. However, in FOWLP the package is fabricated around the good die and fabrication defects will cause good die to be scrapped.