COST COMPARISON FOR FLIP CHIP, WIRE BOND, AND WAFER LEVEL PACKAGING

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ABSTRACT

Wafer level packaging (WLP) is often the most cost-effective approach for achieving miniaturization. However, using wafer level packaging for the wrong applications can be needlessly expensive. The significant differences between printed circuit board interconnect design rules and semiconductor interconnect design rules must be resolved by the package, and this presents unique challenges for wafer level packaging.

If miniaturization is not required, a wire bond package is usually the most cost-effective packaging approach. However, a modified wafer level packaging approach called fan-out wafer level packaging is one option that overcomes the traditional WLP I/O restriction[1]. In many cases, fan-out wafer level packaging or flip chip packaging is the lowest cost solution for applications requiring a moderate number of I/Os with some package size constraints.

This paper compares the total packaging cost of the following four technologies:

- Wire bond packaging
- Flip chip packaging
- Fan-in wafer level packaging
- Fan-out wafer level packaging

The analysis is accomplished using a comprehensive activity based cost model for each of the four package technologies. All wafer preparation activities (bumping for flip chip, wafer mounting, backgrind, dicing, etc.), fabrication activities (redistribution layer creation, inner layer processing, build-up layer processing, drilling, surface finish, testing, singulation, etc.), and assembly activities (die bonding, wire bonding, underfill, mold compound, lid attach, solder ball attach, etc.) are modeled and verified using multiple industry sources.

Keywords: Cost modeling, trade offs, wafer level packaging, flip chip, wire bond

ACTIVITY BASED COST MODELING

Activity based cost modeling and parametric cost modeling are the two dominant cost modeling methods. Parametric cost modeling is done by statistically analyzing a large number of actual results and creating a model that matches as closely as possible. This "black box" approach, as an extrapolation based on historical data, is only appropriate for modeling processes that change slowly over time or cannot be decomposed into individual activities.

For reliable and dynamic trade offs, activity based cost modeling is the most accurate cost modeling method because individual activities are characterized and analyzed. The total cost of any manufacturing process is calculated by dividing the process into a series of activities and totaling the cost of each activity. The cost of each activity is determined by analyzing the following attributes:

- The time required to complete the activity
- The amount of labor dedicated to the activity
- The cost of material required to perform that activity—both consumable and permanent material
- Any tooling cost
- The depreciation cost of the equipment required to perform the activity
- The yield loss associated with the activity

Activity based cost modeling is also well suited to comparing different technologies and manufacturing processes. The total cost of a product can be divided into the following three categories:

- Direct manufacturing cost
- Allocated factory overhead
- Profit margin

The direct manufacturing cost is easy to quantify and reasonably consistent across the industry. However, factory

overhead and profit margin vary significantly between different manufacturing sites and companies. By using activity based cost modeling, the specific differences in manufacturing cost can be determined by comparing the direct manufacturing costs. This "relative" cost modeling makes it much easier to understand the cost impacts—good or bad—of design decisions and technology tradeoffs.

The graph in Figure 1 shows a partial example of an activity based cost graph for a wire bond substrate. Each activity contributes cost in at least one of the six categories shown. These categories are represented by the colored bars, and the running total is the line on the graph. The example shows the first series of activities in a wire bond substrate fabrication process.

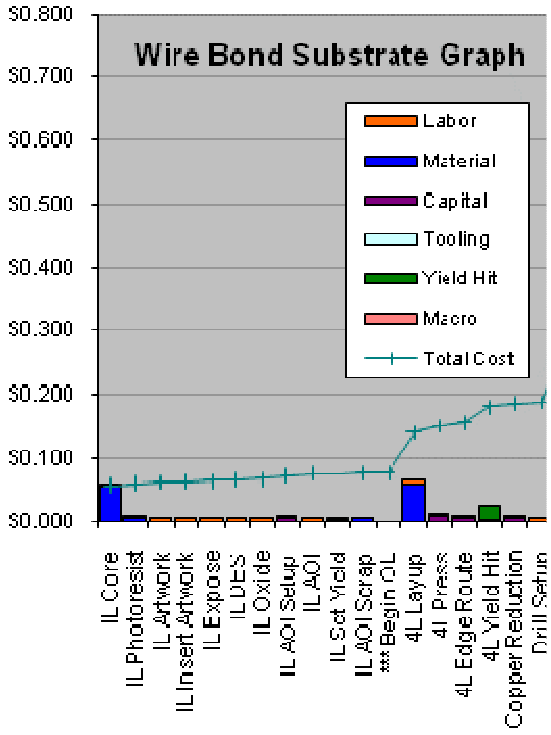


Figure 1. Example of Activity Based Cost Modeling (Partial Cost Graph)

The inner layer contributes a significant material cost as shown by the blue bar labeled "IL Core". Many of the other activities contribute labor and equipment depreciation cost as shown by the orange and purple bars.

WIRE BOND PACKAGING

Wire bond packaging is a mature technology that has been used to package billions of components. Given this maturity, manufacturing efficiency and yields are both quite high.

One of the primary purposes of any package is to convert the semiconductor I/O pad width and spacing into printed circuit board I/O pad width and spacing. Because the design rules are different, this conversion may result in a high cost. For wire bond packaging, this conversion is done during the wire bonding process, which is relatively low-cost. The die I/O pads at a fine pitch are connected to the substrate fingers at a larger pitch. This effectively "spreads out" the I/Os and makes it easy to connect the I/Os from the substrate fingers through the substrate to the PCB.

Consequently, wire bond substrates are simple and inexpensive to build since the wire bonding activity is spreading the I/Os, rather than requiring the substrate to handle the fine pitch semiconductor design rules. A two- or four-layer substrate with no high-density interconnect is usually adequate for most wire bond packages.

One exception is the case of wire bond chip scale packages (CSPs). Unlike normal wire bond packages that have room to spread the wires during wire bonding, the small size of the CSP relative to the die forces more of the I/O design rule conversion to be accomplished in the substrate—thus adding expense[2].

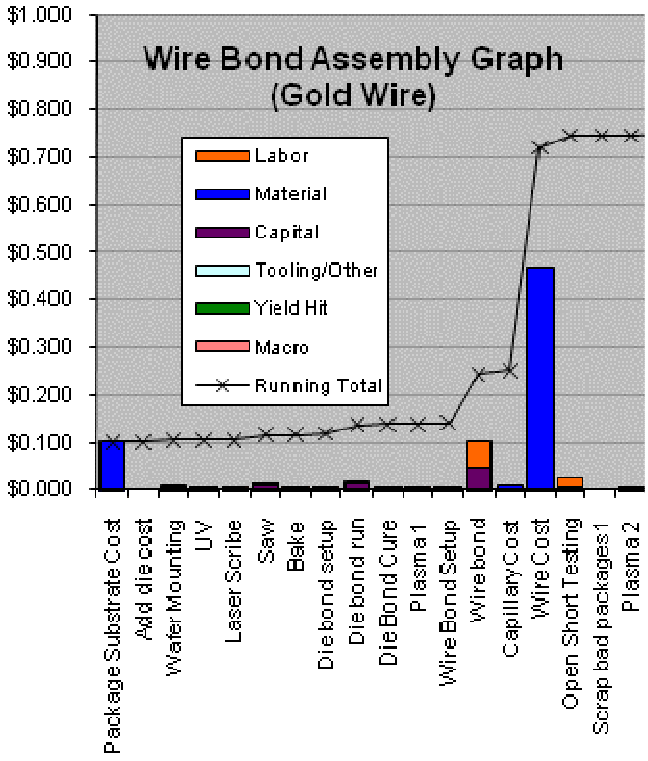


Figure 2. Wire Bond Assembly with Gold Wire (Partial Cost Graph)

While the non-CSP wire bonding activity and substrate are low cost, the cost of gold wire can be expensive. The chart in Figure 2 shows a partial result of the cost details of using gold wire assuming the price of gold is $1,200 per ounce. The design shown in the example is a 12x12mm package with 361 I/Os. The total cost of this package including substrate and assembly is approximately $0.91. More than 50% of the total cost is due to the material cost of the gold wire.

Using copper wire as an alternative to gold has become quite popular. However, today's assembly yield is lower and the wire bonding time is longer due to the stiffness of the copper wire[3].

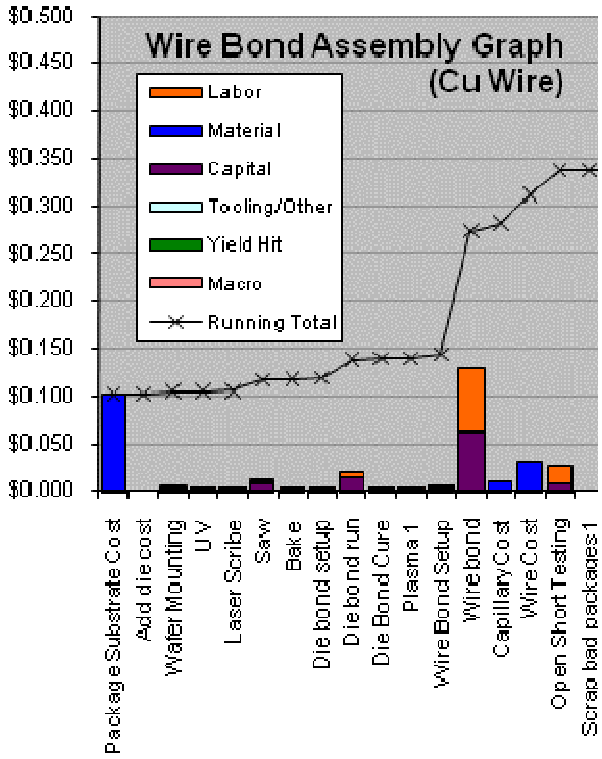


Figure 3. Wire Bond Assembly with Copper Wire (Partial Cost Graph)

The chart in Figure 3 shows the same design with copper wire instead of gold. Even though the cost of the wire bonding activity with copper is greater than with gold (shown by the wire bond activity bar in the graph), the copper wire material cost is low. The total package cost for this design with copper wire is approximately $0.47, which is substantially lower than the original $0.91 with gold wire.

Wire bond packaging is generally the most cost-effective technology if a large package can be used relative to the I/O count and size of the die. Copper wire is the best choice, but in most cases, gold wire can also be cost-effective.

FLIP CHIP PACKAGING

Flip chip packaging using an area array solder bump or copper pillar configuration is rapidly becoming a popular alternative to wire bond packaging. This trend is largely due to thermal and electrical properties, declining cost, its ability to support high I/O count packages, and its ability to support smaller packages relative to the die size[4]. As shown in Figure 4, the connection area required for flip chip is much smaller than that required for wire bonding because all of the I/Os from the chip are connected through the bottom of the chip. Packages that are smaller in relation to the size of the die can be achieved.

However, this smaller area comes at a cost. The two major cost drivers for flip chip packaging are both directly related to the act of bringing the I/Os out under the die. The first major cost driver is bumping the wafer. Die pads are designed in an area array format, and the wafer is bumped for connection to the substrate. This bumping may be solder bumps or copper pillar, but either technology is a significant cost driver.

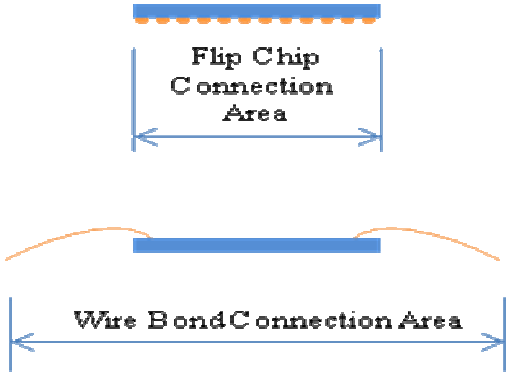


Figure 4. Wire Bond versus Flip Chip I/O Connection Area

The second major cost driver is the substrate. This cost comes from a combination of the high connection density, fine pitch design rules, and the fact that a significant number of build-up layers for escape routing are required to connect to the die.

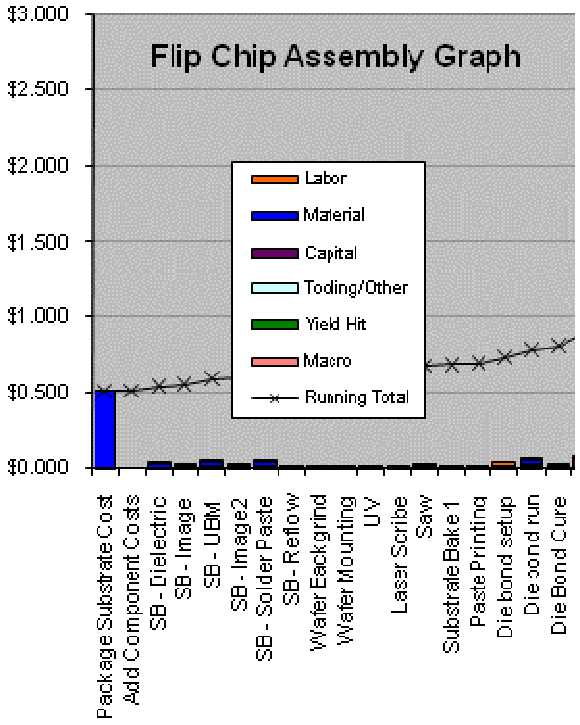


Figure 5. Flip Chip Assembly Graph (Partial Cost Graph)

The cost graph in Figure 5 shows the same example used in the wire bond scenario (12x12mm substrate with 361 I/Os). In this case, the total packaging cost is approximately $2.73, compared to $0.91 (or less with copper) for a wire bonding solution. Of this $2.73, more than $0.65 is due to the substrate and to wafer bumping.

WAFER LEVEL PACKAGING

Traditional WLP is sometimes referred to as fan-in wafer level packaging. Once the semiconductor wafer is fabricated, the additional processing to complete wafer level packaging is straight forward and easily accomplished in the same factory. Therefore, WLP is usually a single manufacturing process that begins with a wafer and ends with a "ready to ship" packaged chip. In contrast, a chip packaged with wire bond or flip chip technology requires three different manufacturing processes: fabrication of the semiconductor, fabrication of the package substrate, and assembly of the die on the substrate. These processes are distinct and not suitable for completion in one factory.

In addition to the straight forward manufacturing process for fan-in WLP, another major advantage is package size. Since the package is fabricated directly on the wafer, the package and the die must be the same size after singulation. Size is also an advantage in terms of height; wafer level packaging results in a low profile package, which can be beneficial in many applications.

However, fan-in wafer level packaging presents a substantial disadvantage for any application requiring even a moderate number of I/Os. As discussed in the flip chip section, one of the major roles of any semiconductor package is to convert the semiconductor I/O design rules into printed circuit board I/O design rules. Since the PCB I/O design rules are much looser than those for the semiconductor, the number of I/Os possible from the package is quite low compared to the number of I/Os possible from the die. Increasing the I/O count by growing the die or using fine pitch PCB design rules can significantly increase the cost.

One way to capture the benefits of wafer level packaging and overcome that I/O restriction is to use an approach called fan-out wafer level packaging. Instead of directly fabricating the package on the semiconductor wafer, the wafer is diced and the individual die are placed in a different substrate before the wafer level packaging steps are performed. This allows the fan-out wafer level package to be larger than the die and therefore support a higher number of I/Os.

Fan-out WLP has an advantage over traditional wire bond and flip chip packaging in that only two distinct manufacturing processes (semiconductor and fan-out wafer level packaging) are required to complete the product. However, it is not as straight forward as the one process for traditional wafer level packaging. The diagram in Figure 6 shows the expanded I/O capacity of a fan-out WLP.

Figure 7 is an example of a fan-in WLP process flow for a 5x5mm die and package. The total cost of this package is approximately $0.09.

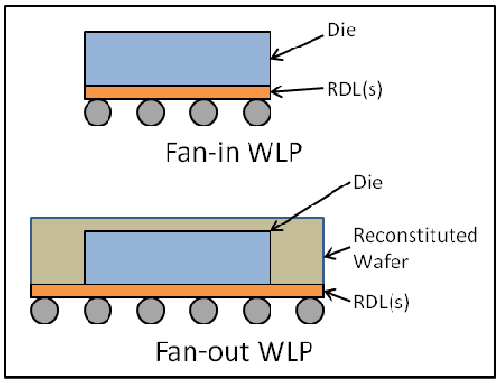


Figure 6. Fan-in versus Fan-out WLP

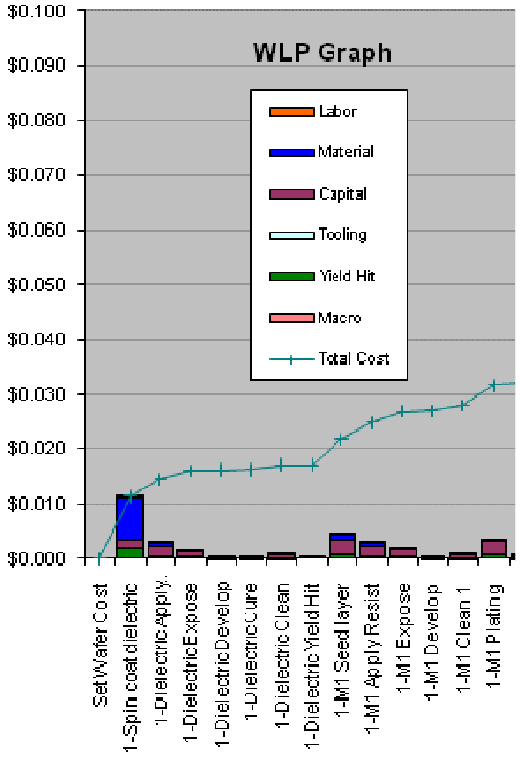
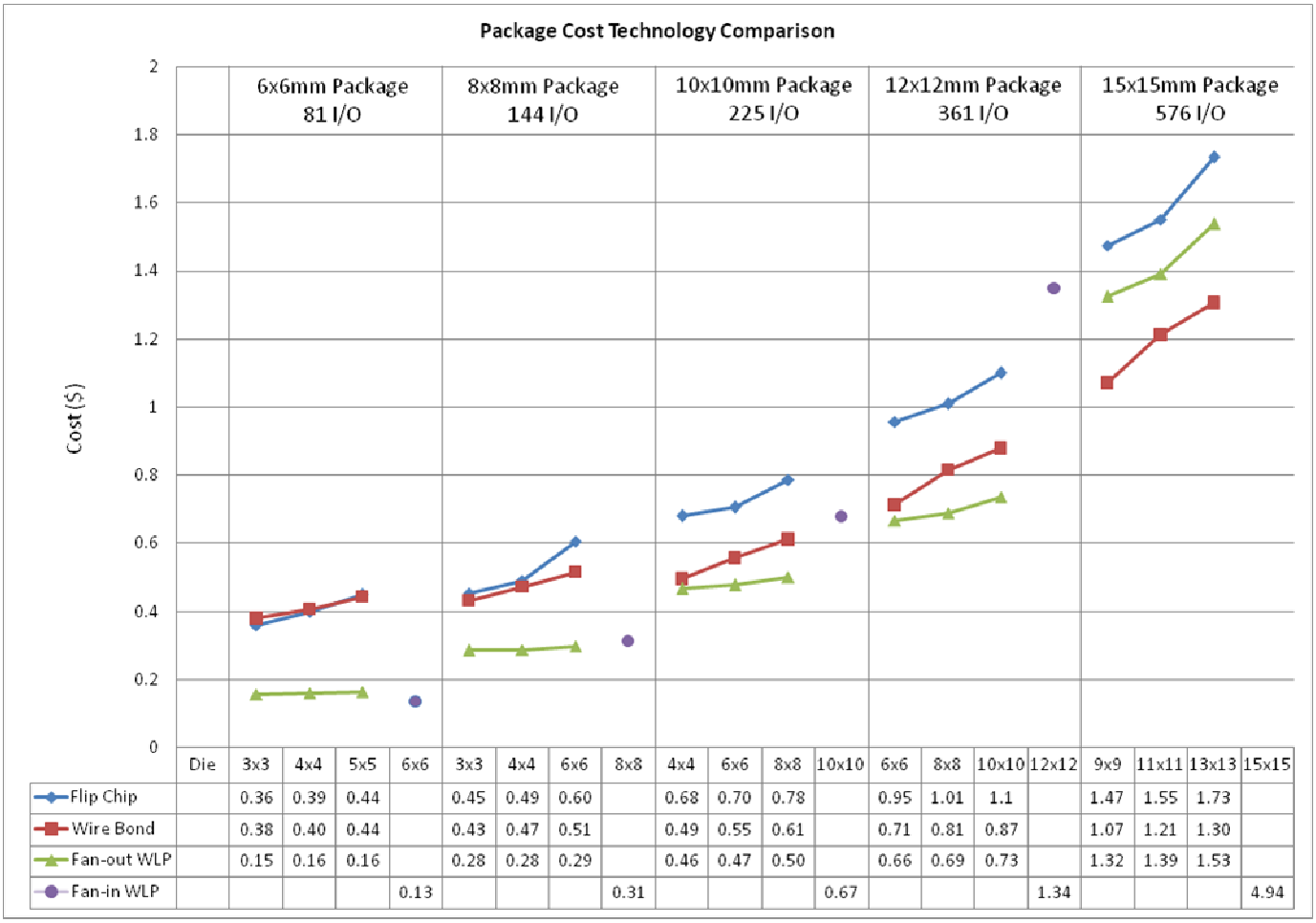


Figure 7. WLP Cost Graph (Partial Cost Graph)

Wafer level packaging and flip chip packaging are both good solutions for miniaturization. The advantages with WLP are that no wafer bumping is required, and it is much simpler to fabricate the package to match the semiconductor design rules since the process is primarily a semiconductor process. The disadvantage is limited package size and I/O count (even with fan-out) due to the fact that a semiconductor process is used for everything. Large, high I/O count packages are more cost efficient if built using a 20x24 inch (approx. 508x610mm) PCB panel rather than a 12 inch (approx. 300mm) semiconductor wafer.



Die	3x3	4x4	5x5	6x6	3x3	4x4	6x6	8x8	4x4	6x6	8x8	10x10	6x6	8x8	10x10	12x12	9x9	11x11	13x13	15x15
Flip Chip	0.36	0.39	0.44		0.45	0.49	0.60		0.68	0.70	0.78		0.95	1.01	1.1		1.47	1.55	1.73	
Wire Bond	0.38	0.40	0.44		0.43	0.47	0.51		0.49	0.55	0.61		0.71	0.81	0.87		1.07	1.21	1.30	
Fan-out WLP	0.15	0.16	0.16		0.28	0.28	0.29		0.46	0.47	0.50		0.66	0.69	0.73		1.32	1.39	1.53	
Fan-in WLP				0.13				0.31				0.67				1.34				4.94

Figure 8. Package Cost Technology Comparison

PACKAGE COST COMPARISONS

The graph in Figure 8 shows a cost comparison of four packaging technologies applied to different package and die sizes. Each segment of the chart represents a different package size, and the four data points within the segment are different die sizes. All cases use a BGA pitch of 0.6mm; flip chip, wire bond, and fan-in WLP scenarios were run on all die sizes up to 1mm less than the package size. In many cases, it is possible to use flip chip and wire bond technology for chip scale packages that are less than 1mm larger than the die, but those costs can be higher, particularly for wire bond technology since the connections all must be made in the area between the edge of the die and the edge of the package.

Flip chip package costs are shown in blue in Figure 8. There are two dominant cost drivers for flip chip packages. The first is the cost of the substrate. In this example, we assumed a 3-2-3 substrate structure for the smallest die in each package, a 2-2-2 structure for the second smallest die, and a 1-2-1 structure for the third smallest die. These assumptions are a direct result of the diagram in Figure 4. The worst case for a flip chip substrate is a small die because the substrate I/Os must all be within the die area. A larger die is easier to connect and therefore does not require a complex layer stack-up for the substrate.

The second major cost driver is the wafer bumping. In this case, a large die is more expensive because wafer bumping is a cost per area. Since the packaging cost of increasing die sizes within the same package increases in all cases, the additional cost of wafer bumping larger die adds more cost than the savings associated with using a simpler substrate.

Wire bond packaging costs are shown in red in Figure 8. The two major cost drivers for wire bond packaging are the substrate cost and the wire bonding cost. Again referencing Figure 4, a simple substrate technology is used for the smallest die in each package, while a more complex substrate is used when the size of the die approaches the size of the substrate. For each package, a two layer substrate is used for the smallest die, a four layer substrate is used for the second smallest die, and a 1-2-1 substrate is used for the third smallest die. Gold wire with a diameter of 1 mil is used in all cases. While the cost of wire bonding continually increases with larger packages, it does so at a slower rate than the alternatives. For a 15x15mm package, wire bond packaging has a clear cost advantage over the other technologies

Fan-out WLP costs are shown in green in Figure 8. For all die sizes in the 6x6mm and 8x8mm packages, there is a significant cost advantage. However, the cost of fan-out WLP is much higher for larger packages. This is largely due

to the fact that fan-out WLP technology is a semiconductor process, as opposed to flip chip and wire bond packaging which is primarily a printed circuit board (PCB) process. PCB processes use a large fabrication panel compared to the wafer used for a semiconductor process. For small packages, the wafer versus panel size difference is not as significant as with large packages.

The fan-in WLP costs are shown in purple in Figure 8. There are only five data points on the graph since the package size and the die size must be the same. Fan-in WLP is the lowest cost solution for a 6x6mm package, and is close to the lowest cost for an 8x8mm package. However, fan-in WLP is not cost effective for packages larger than 12x12mm. The cost problem with large packages for fan-in WLP is primarily due to the fact that the fan-in WLP manufacturing process has no testing and scrapping until the end. Large die have a lower yield, and the fan-in WLP process further reduces yield. Since small die generally have a much higher yield, the compounding yield problem is not a significant cost adder for small packages.

SUMMARY AND CONCLUSIONS

Based on the technology cost modeling and cost drivers presented in this paper, we can draw the following conclusions.

WLP, particularly fan-in WLP if the I/O count is small enough, can be the most cost effective packaging solution for small packages. As shown in Figure 8, both wafer level packaging technologies display a significant cost advantage over flip chip and wire bond solutions for packages less than 8x8mm.

Wire bond packaging is usually the most cost effective solution for large packages if the I/O count is reasonable. Wire bond packaging is extremely cost effective, but a substantial area is required for the wire bonding. Therefore the number of I/Os must not be too large or there will not be enough room between the die and the edge of the package for the wire bonding.

Either fan-out WLP or flip chip technology tends to be the most appropriate solution for moderate to large CSP packages. In many cases requiring a CSP, the die is too large or the I/O count is too high for either wire bond or fan-in WLP. However, both flip chip and fan-out WLP connect to the substrate using the area under the die. Since no connections are made around the periphery of the die, the die and the package can be close to the same size.

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