A TECHNOLOGY TO REDUCE PAD CRATERING DEFECTS AND THE IMPACT ON PRODUCT COST

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ABSTRACT

While any printed circuit board manufacturing defect is expensive, pad cratering defects are particularly costly. These defects are almost impossible to rework, and they are usually detected at the end of the process. All components, the PCB, and the cost of fabricating and assembling the board is scrapped. An even worse situation than finding the defect at the end of the process is not detecting it at all. This leads to even more expensive customer failures and product returns.

In this paper, we describe a technology and manufacturing process which reduces pad cratering defects. A complete product cost analysis of this process, including breakeven and sensitivity analysis, is carried out using activity based cost models.

Keywords: Cost modeling, pad cratering, PCB fabrication cost

INTRODUCTION

Pad cratering defects are failures of the SMT solder pad on a printed circuit board [1]. They are typically stress induced and are happening more frequently due to higher processing temperatures and brittle dielectric associated with lead free soldering requirements [2].

The addition of Zeta® Cap material to the PCB fabrication process reduces the number of pad cratering defects. Adding this material increases the material component of the product cost, but if the cost associated with yield loss is reduced, total product cost may be less [3].

ACTIVITY BASED COST MODELING

Activity based cost modeling and parametric cost modeling are the two dominant cost modeling methods. Parametric cost modeling is done by statistically analyzing a large number of actual results and creating a model that matches as closely as possible. This "black box" approach, as an extrapolation based on historical data, is only appropriate for modeling processes that change slowly over time or cannot be decomposed into individual activities.

For reliable and dynamic trade-offs, activity based cost modeling is the most accurate cost modeling method because individual activities are characterized and analyzed. The total cost of any manufacturing process is calculated by dividing the process into a series of activities and totaling the cost of each activity. The cost of each activity is determined by analyzing the following attributes:

- The time required to complete the activity
- The amount of labor dedicated to the activity
- The cost of material required to perform that activity—both consumable and permanent material
- Any tooling cost
- The depreciation cost of the equipment required to perform the activity
- The yield loss associated with the activity

Activity based cost modeling is also well suited to comparing different technologies and manufacturing processes. The total cost of a product can be divided into the following three categories:

- Direct manufacturing cost
- Allocated factory overhead
- Profit margin

The direct manufacturing cost is easy to quantify and reasonably consistent across the industry. However, factory overhead and profit margin vary significantly between different manufacturing sites and companies. By using activity based cost modeling, the specific differences in manufacturing cost can be determined by comparing the direct manufacturing costs. This "relative" cost modeling makes it much easier to understand the cost impacts—good or bad—of design decisions and technology tradeoffs.

The graph in Figure 1 shows a partial example of an activity based cost graph for a high density interconnect (HDI) PCB substrate. Each activity contributes cost in at least one of the six categories shown. These categories are represented by the colored bars, and the running total is the line on the graph. The example shows the first series of activities in the fabrication process.

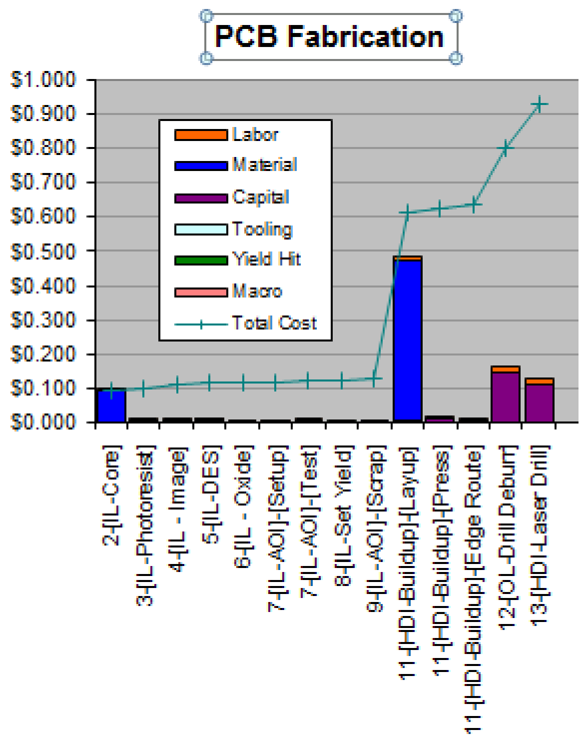

Figure 1. Example of Activity Based Cost Modeling (Partial Cost Graph)

The inner layer core and HDI buildup activities contribute a significant material cost as shown by the blue bar in those two steps. Any type of via drilling—either laser or mechanical—will contribute capital costs since the throughput per panel is usually low. Many of the other activities contribute labor and equipment depreciation cost as shown by the orange and purple bars.

PAD CRATERING

Pad cratering is defined by IPC-9708 [4] as "the formation of a cohesive (or adhesive) dielectric crack or fracture underneath the pad of a surface mount component, most commonly BGA packages." When the fracture propagates through the copper trace or connecting via, an open circuit is created. Fractures are sometimes detected when an assembled PCB is electrically tested. A microsection of such an open pad is shown in figure 2.

Fractures in the dielectric (resin) under the PCB pad are not new, but a combination of higher lead free solder temperatures, higher modulus solder joints and temperature resistant but brittle resin systems increase the risk.

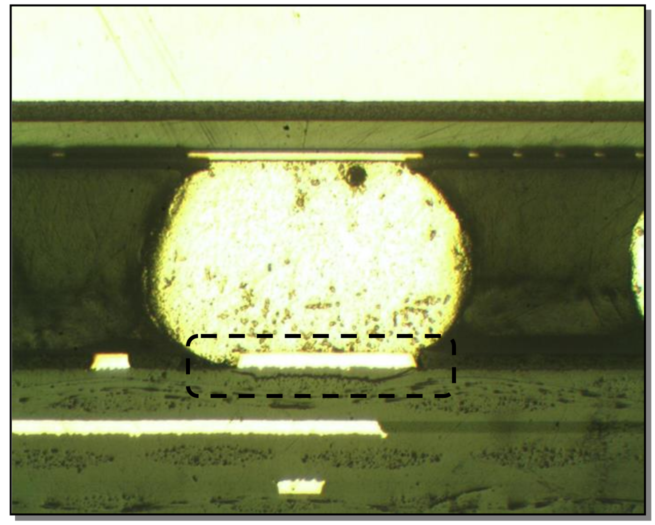

Figure 2. Example of a Pad Crater (Fracture under Pad)

A MATERIAL APPROCH

A thin layer is applied that is different in composition from the rest of the PCB structures. The properties of this layer can be adjusted to provide both a fracture barrier and a stress relief. Figure 3 shows this layer (Zeta® Cap) supporting the surface pad.

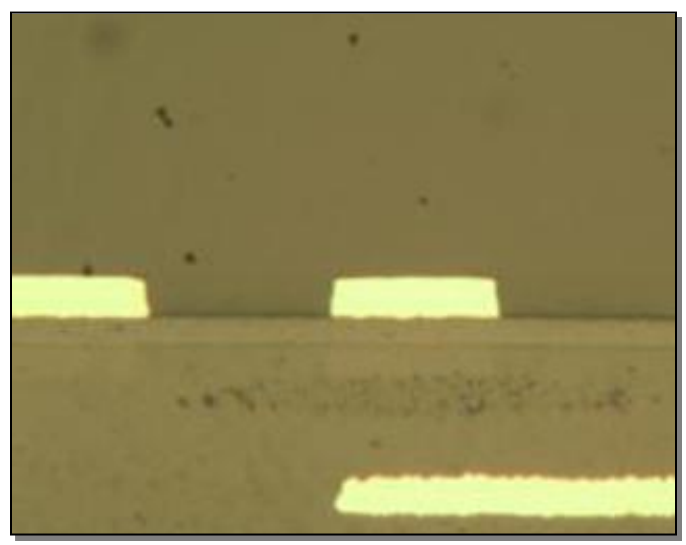

Figure 3. Zeta® Cap layer

This layer has a relatively high elongation compared with other high temperature resins while retaining a medium modulus. A material like this is not practical to use for the entire structure (due to its very high cure temperature), but it can easily be applied to the surface directly supporting the BGA pads. Figure 4 shows an assembled PCB with the Zeta ® material.

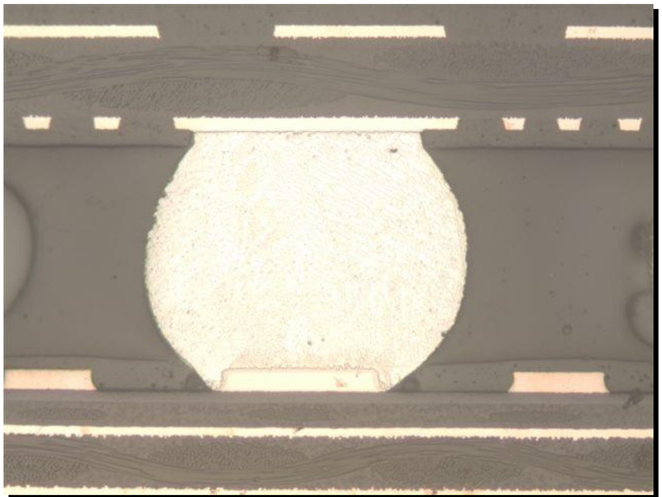

Figure 4. Assembled PCB with Zeta® Cap

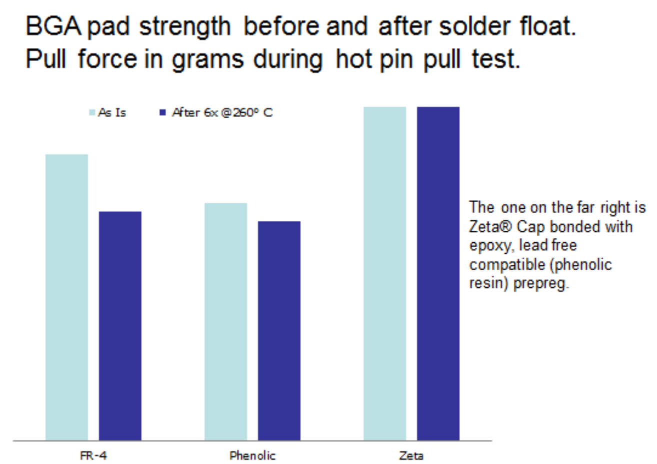

Figure 5. Hot pin pull test results

Figures 5 and 6 show hot pin pull and inflection strain test results using a thin layer of Zeta® Cap (25 microns) on a lead free compatible laminate.

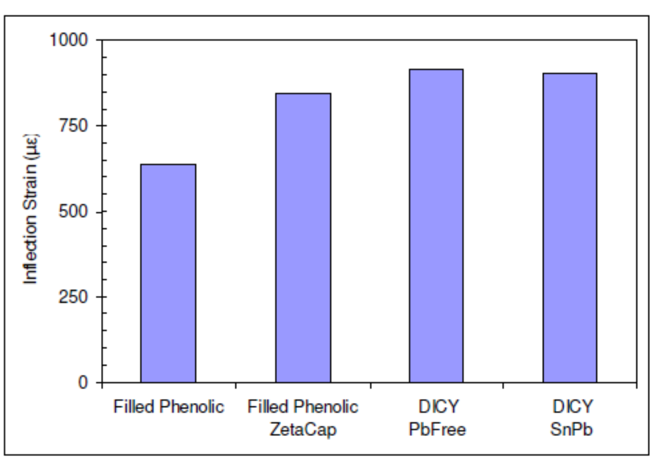

Figure 6. Inflection strain test results

This thin layer restores the PCB to the same pliant conditions observed when not using lead free solder and more brittle laminates.

COST MODELING RESULTS

Two designs were analyzed to determine the cost impact of using Zeta® Cap on the top and bottom layers as compared to a baseline without Zeta® Cap. To cover different levels of complexity and design density, a typical cell phone board and server board were selected as the two designs for analysis. The properties of these boards are outlined in Table 1.

Table 1 – Example Designs

Cell Phone	Server
2 x 2.5 inch	18 x 24 inch, 1 up design
8 layer board, 3-2-3 structure	22 layer board, no HDI
371 SMT components, 0 TH components	2410 SMT components, 35 TH components
All manufacturing using Taiwan labor rates and high volume production	All manufacturing using Taiwan labor rates and medium volume production
Assembly panel is 4 boards, Xouts are allowed. High volume balanced factory	Assembly panel is 1 board.
Total component cost of $106.55	Total component cost of $398

For the mobile phone design, it is assumed that Zeta® Cap improves the assembly yield by 7.08%, which is equivalent to 60 DPMO per solder joint; for the server, the assumed improvement is 2.0%, which is equivalent to 15 DPMO per solder joint. Underfill of three ASICs is included in the baseline cost of the mobile phone design, and no underfill is performed when Zeta® Cap is used on the board since it is not required with the use of Zeta® Cap. A 25% rework success rate for failure due to pad cratering defects is assumed for both boards, and scrap costs only include failures found during manufacturing test. While most pad cratering failures cannot be reworked, a 25% success rate was used to account for the cost recovered by harvesting good components. Field failures and return costs are not included in this analysis.

The following two tables summarize the cost model results. The results are broken down into multiple categories, and comments about the specific changes between the two cases, if any, are included.

Table 2 – Mobile Phone Cost Model Results

	Baseline Case	Zeta® Cap Case	Comments
PCB Cost	$5.21	$5.83	Extra material cost of 1 layer of Zeta® Cap on top and bottom minus process savings
Component Cost	$106.55	$106.55	No change in two cases
Assembly and Test	$3.60	$2.25	Extra cost of underfill and component harvesting
Scrap due to pad cratering yield loss	$6.92	$0.00	Change due to pad cratering defect removal
Assembly Yield	92%	99%	
TOTAL	**$122.28**	**$114.63**	
Note: Zeta® Cap case has 99% assembly yield and baseline case has 92% assembly yield. The lower yield design has extra cost associated with rework and scrap.			

Table 3 – Server Cost Model Results

	Baseline Case	Zeta® Cap Case	Comments
PCB Cost	$227.450	$284.680	Replace foil on top and bottom with 1 layer of Zeta® Cap minus 2% yield improvement
Component Cost	$398.313	$398.310	No change in two cases
Assembly, Test, and Rework	$37.251	$28.850	Extra cost of underfill and component harvesting
Scrap due to pad cratering yield	$78.952	$0.000	Change due to pad cratering defect removal
TOTAL	**$741.966**	**$711.840**	

SENSITIVITY AND BREAK EVEN ANALYSIS

Both cases in the previous section are presented as a snapshot of a particular design using the specific assumptions listed.

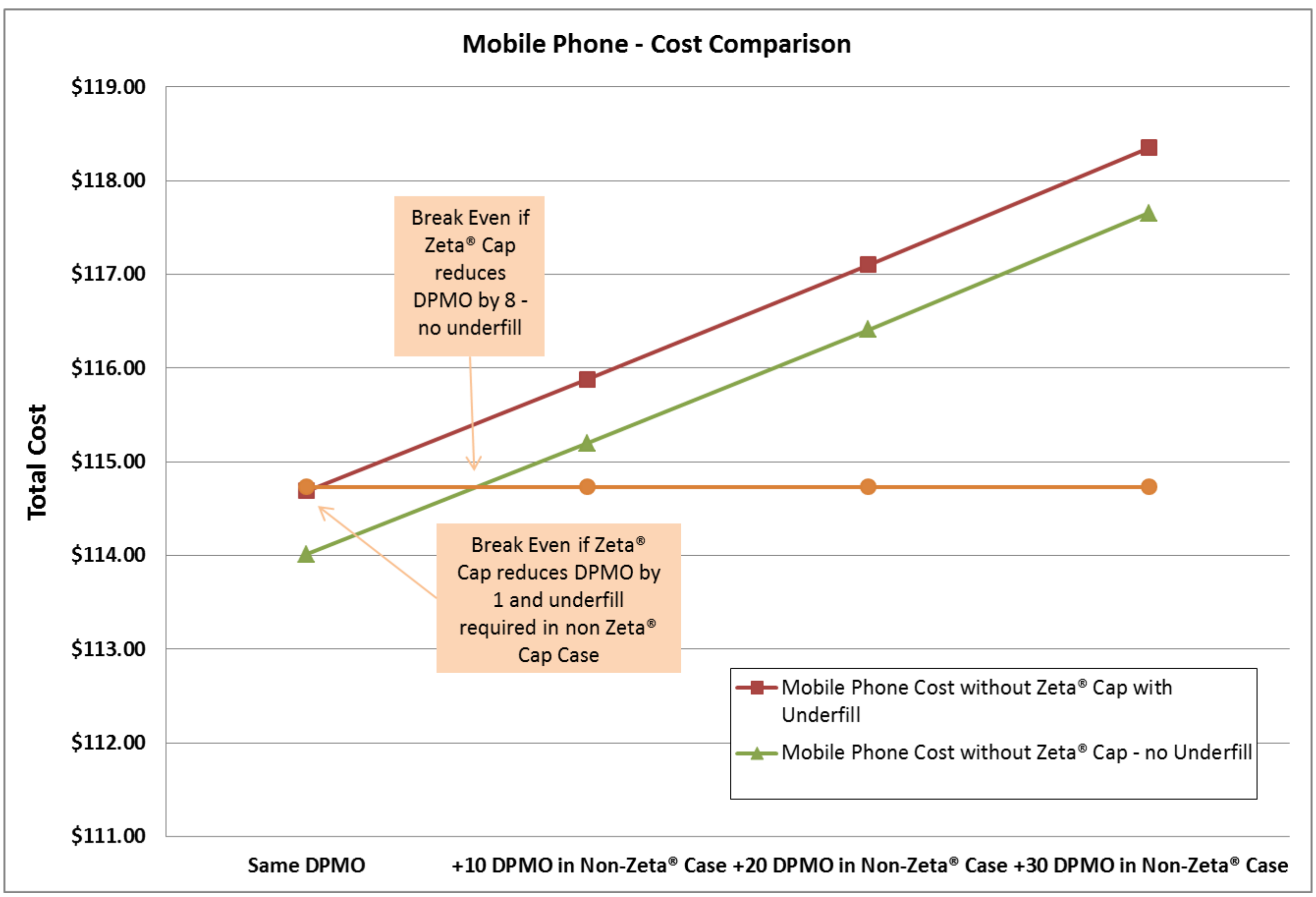

Figure 7. Mobile phone sensitivity and break even analysis.

However, more detailed analysis is required to fully understand when the specific benefits of Zeta® Cap can be achieved. Further sensitivity analysis was carried out on each board to determine the break even point—that is, the amount of improvement required to make the cost of using Zeta® the same as the cost without using Zeta®.

Including Zeta® Cap during board fabrication reduces the probability of pad cratering defects. This probability can be expressed in terms of defects per million opportunities, or DPMO. The mobile phone graph below shows that the total cost using Zeta® Cap will be the same as not using Zeta® Cap if pad cratering defects are reduced by 8 DPMO and all other conditions are kept the same. If underfill is added to the non-Zeta® Cap case to minimize pad cratering defects, Zeta® Cap only needs to improve the defects by 2 DPMO to break even.

In the server scenario, the break even point occurs if Zeta® Cap reduces the defects by 8 DPMO. For each case, if the use of Zeta® Cap reduces the defects by more than 8 DPMO, the product with Zeta® Cap will be less expensive.

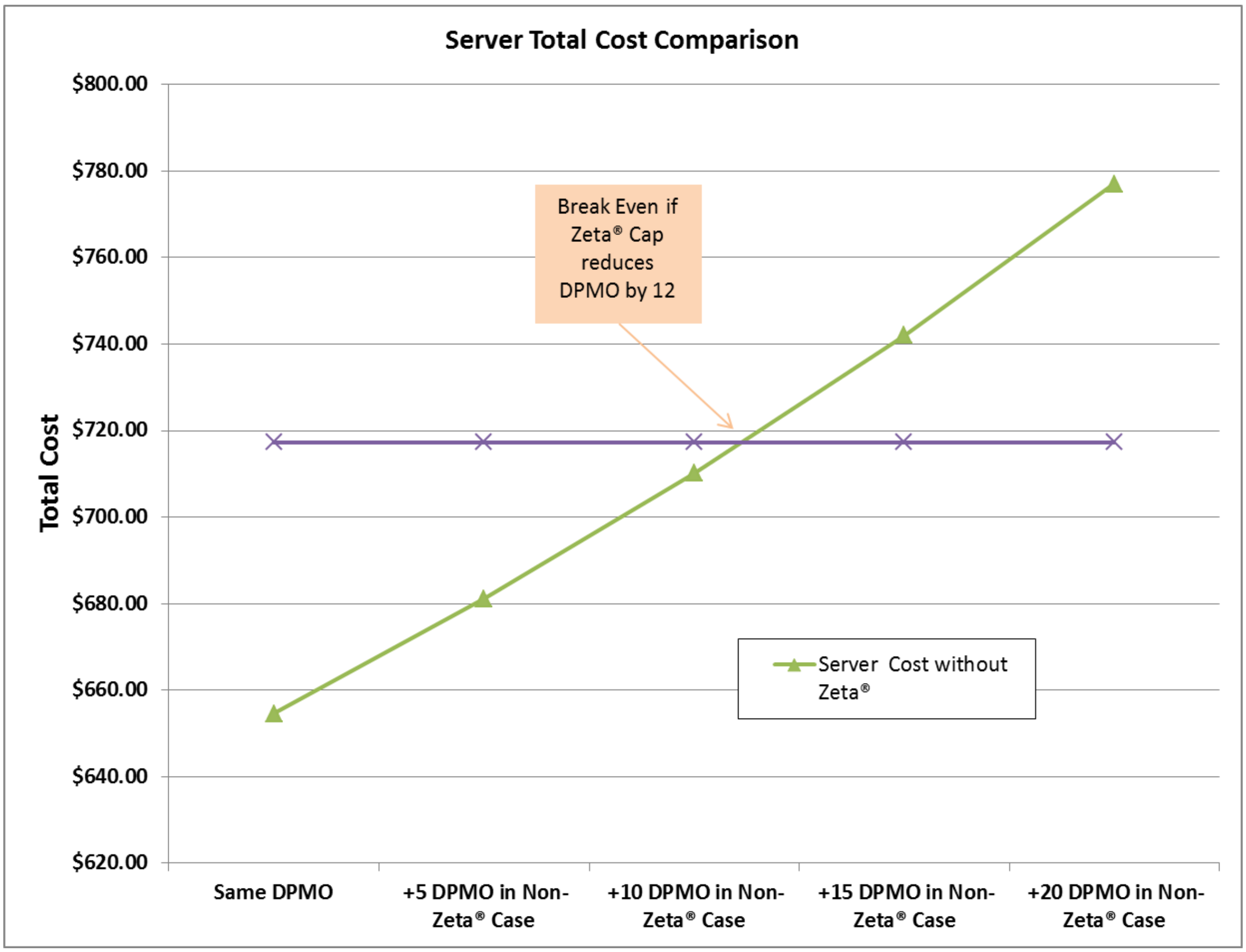

Figure 8. Server sensitivity and breakeven analysis.

SUMMARY

Activity based cost modeling was used to explore the benefits of using Zeta® Cap to reduce pad cratering defects. In addition to looking at the total cost breakdown of specific designs, sensitivity yield analysis was used to determine the break even point for multiple designs. The following conclusions can be drawn.

- **Pad Cratering defects can be reduced by adding a material beneath a surface mount pad.** This purpose of this material is to provide stress relief and to limit fracturing.
- **The additional cost of adding Zeta® Cap to the board fabrication process is offset if the probability of pad cratering defects is reduced by at least 8 DPMO in the two cases shown.** The exact yield improvement will vary for other situations, but given the high cost of scrap pad cratering that is present, only a modest yield improvement is required for Zeta® Cap to be the lowest cost option.

REFERENCES

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