Activity Based Cost Modeling for Embedded Passives

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Abstract
This paper identifies the key differential cost drivers of embedded passives versus discrete passives. It also compares and contrasts two different cost modeling methods. A simple parameter based approach is compared to a detailed activity based modeling approach. The simple parameter based approach has poor accuracy, but has a small initial set up cost since many cost drivers are ignored. This approach is useful in deciding whether to rule out embedded passives from consideration for a specific design. The activity based modeling approach provides the required accuracy to understand the true cost differences for the design and should be used prior to committing to the technology for that design. This approach is just as easy to use as the simple parameter based approach after a one time initial model creation activity. Finally, an overview of design characteristics suitable for cost effective embedded passives is presented.

Embedded Passives Cost Overview
The cost tradeoffs associated with the manufacture and assembly of boards containing embedded passives is complicated by differences in board fabrication and board assembly. This means the cost drivers associating with embedding passives are spread throughout the supply chain, making it extremely difficult to compare options.

The cost differences which span the fabrication and assembly process are also difficult to determine and maintain due to the following three points:

1. Wide variation of the costs involved – The component costs, board fabrication costs, and assembly costs vary greatly. Large OEMS typically have corporate contracts with board shops and contract manufacturers resulting in their actual costs being very different from smaller companies. Component costs also vary greatly based on volume purchase contracts which have nothing to do with the specific design being considered. Because of this wide variation, it is not appropriate to use some industry average number.

2. Confidentiality of the costs involved – The actual cost of a material or process is usually considered highly confidential. Because of this confidentiality, suppliers may publish an average price that they charge, and it will often be higher than the true average. (Nobody wants to publicize a price that is lower than what they charge any of their customers.) Using average published numbers makes it difficult to get an accurate model for a specific design.

3. Fluidity of the costs involved – The costs associated with both discrete passives and embedded passives change rapidly. Therefore, any model that relies on these costs must be continually updated. These changes are not only due to technological advances, but economic factors as well. Board fabricators and contract manufacturers faced with a lot of excess capacity will charge less than they would if they were capacity constrained.

Manufacturing Cost Drivers
In order to conceptually understand the difference between the cost of a board with embedded passives and the cost of the same board using discrete passives, it is helpful look at which costs are affected, and the rate at which they change. For example, adding two discrete capacitors to a design will cost twice as much as adding one discrete capacitor. However, the cost of two embedded capacitors on a board is the same as the cost of one embedded capacitor, because the cost of a capacitive layer pair is incurred on a per panel basis, not per device. The cost drivers for embedded passives can be grouped into the following three categories:

1. Increased board fabrication cost – The primary drivers that increase the board fabrication cost when embedding passives are increased material costs and the addition of extra processing steps. Most of the cost associated with the extra processing steps is incurred on a per panel basis. For example, the cost of adding a layer pair with a thin dielectric for embedded capacitors is the same whether there is one embedded capacitor on the panel or 10,000. However, some processing steps do have a substantial cost per device component as well as a cost per panel component. For example, the extra cost associated with laser trimming resistors contains a small cost that is independent of the number of resistors to be trimmed, as well as a larger cost that is dependent on the number of resistors trimmed. The location and the layout of the design also have a large influence on

the cost per trimmed resistor. The net result is that these costs are heavily design dependent.

While most of the extra processing costs are driven on a per panel basis, some of the extra material costs are driven on a per device and per panel basis. As noted above, the extra material cost for an embedded capacitance layer pair is purely per panel. However, the material cost for ceramic devices and the ink for printed devices vary based on the number of devices.

2. Decreased board assembly and component cost – Since the embedded devices replace discrete devices, the cost of assembling the board is reduced. The direct cost improvements include the cost of the replaced components plus the cost of placing those components on the board. Additionally, a board with embedded devices will have higher yield and reliability due to fewer solder joints. A significant reduction in the board assembly cost may be achieved for boards that can be converted from a two sides to a single side.

3. Decreased board size/cost – In many cases, the surface real estate for placing components is the limiting factor on board size. In these designs, the use of embedded passives may result in a smaller board. If the size reduction is enough to yield more boards per panel, the board fabrication cost of the embedded design may be less than the non-embedded option even though the cost per square inch of embedding is higher.

Embedded Passives Cost Modeling

Given the complexity and the broad scope of the cost drivers surrounding embedded passives, developing a simple and accurate cost model is extremely difficult. By using a number of parameters such as cost per discrete, material cost for embedded devices, etc., a simple cost model can be developed in a spreadsheet. Unfortunately, any simple model will not be accurate for two primary reasons.

1. There are a large number of cost drivers related to design, assembly, and fabrication which significantly affect the result. - In many cases, the obvious drivers such as component costs, placement costs, and material costs are not the dominant factors contributing to the real cost of the board. Instead, the board cost may be dominated by changes in board size, differences in assembly yield, changing from a two sided board to a one sided board, etc. Since the dominant drivers vary on a case by case basis, none of them can be ignored.

2. The drivers vary so broadly that there is no industry average. - Even if many cost drivers need to be considered, a simple model could be created if the costs involved were common across the industry. Unfortunately, they are not. For example, cost per placement may range from one half cent to five cents per discrete. The assembly and fabrication yield can also vary greatly, and if designers do not consider these variations, they will often choose the wrong technology for their design.

Achieving necessary accuracy results in a parameter based model that is complicated and requires a lot parameters. This creates yet another problem for a designer attempting to make the right technology decision. Designers typically do not know the value of many of these parameters. Contract manufacturers will provide system designers with a price quote for a board, but typically will not provide an accurate cost per discrete placement number. Similarly, board fabricators will do a price quote for a board, but they will usually not publish their material costs for the embedded material.

Activity Based Cost Modeling

An approach which overcomes the problems inherent in parameter based modeling of embedded passives is to develop and apply activity based manufacturing models to the board assembly and fabrication process. These models can be extremely accurate since they are structured to include all the cost drivers associated with assembly and manufacturing of boards with discrete and embedded passives (material, yield, size, labor, equipment, overhead, profit margin, etc.). Each activity in the flow is defined and characterized based on the specific manufacturing environment, and the activities are accumulated to define the process model. This cost modeling approach has two main advantages over parameter based modeling:

1. Improved accuracy vs. simplicity tradeoff - As noted previously, if enough parameters are included to provide good accuracy, the operation of the model becomes too complex and probably will not be used. Or, if used, it will be used with the wrong parameters, which is worse than not using it at all. The only alternative is a simple but inaccurate model.

2. The parameters are embedded in the model and designers are not asked questions that they cannot answer. - Whether the cost modeling is parameter based or activity based, the cost drivers are the same. However, during the tradeoff process, instead of a designer being asked to provide the cost per placement of a discrete, he or she merely loads the model for the target manufacturing environment.

A variety of activity based embedded passives cost models have been built and used for tradeoff analyses

using the *SavanSys* technology described in the next section.

The *SavanSys* ™ Technology

Below is a brief description of the *SavanSys* activity based cost modeling technology. For additional information on the capabilities and availability of this technology, please contact the author.

SavanSys is a cost modeling and technology tradeoff tool. Data is extracted from the design tool environment to create a physical representation of the design. Activity based models of both board fabrication and assembly are created to model the manufacturing process. This combination of design and manufacturing information is used to generate a "virtual prototype" of the board to accurately determine size, cost, and yield. The results of this model are extremely accurate because it considers the details of the target board applied to a specific manufacturing environment with accurate costs and yields.

The data considered by *SavanSys* for doing this analysis is listed below.

The Design Model in SavanSys

Because of the substantial number of packaging technologies, processes, and materials that are available, making optimum choices is not a trivial task. Alternative technologies and materials include:

- Substrates (printed circuit boards, ceramic, thin-film, etc.)
- Chip packaging
- Bonding techniques (wirebond, TAB, flip chip)
- Test techniques
- Manufacturing methods

SavanSys accepts physical information that describes multiple chips (or bare die) and their interconnection. All of the information that is collected by *SavanSys* is physical, as opposed to logical, behavioral, or functional. *SavanSys* does not import VHDL or similar behavioral information because such descriptions do not contain a significant amount of useful physical information. *SavanSys* accepts the following physical inputs.

Chips (bare die and packaged die):

- Dimensions (length, width, thickness)
- I/O type and count
- Cost and yield

Chip Packaging:

- Bonding (technology, materials, and design rules)
- Encapsulation (materials and design rules)
- Die attach (materials and design rules)
- Process flow information (chip preparation, testing, and burn-in)

Boards/Modules:

- Substrate (technology, materials, and design rules)
- Connectorization (technology, materials, and design rules)
- Process flow information (substrate fabrication)

In *SavanSys*, netlists are optional because tradeoff activities often take place prior to the presence of a detailed netlist. Therefore, the total number of nets in a partition can be estimated with *SavanSys* even without a detailed netlist.

Module size prediction is accomplished by computing the following set of footprints for each component (active and passive) in the board.

- The interconnect-capacity footprint is the size limitation based on the amount of wiring required to connect a component within the module. It depends on the wiring capacity of the substrate and the quality of the routing.
- The via-density footprint accounts for the number of vias that are available to connect component I/O to wiring layers.
- The bond-pad-density footprint accounts for the distribution of bond pads on the surface of the interconnecting substrate.
- The escape-routing footprint analyzes routing component I/O out from under the die, either to wiring tracks on the surface of substrates or to vias that connect to other wiring layers.
- The placement or die footprint represents the physical size of the bare die or packaged chip and its surrounding bonds, as well as minimum spacing to adjacent components.

In order to obtain the module area, the footprints representing each component are appropriately accumulated.

The Manufacturing Model in SavanSys

SavanSys cost models may include the following costs. Since the costs below are optional, *SavanSys* models can be used to analyze total system costs or specific components of the system cost.

- Component costs (entered or computed)
- Component preparation (process may be defined)
- Single chip package costs (entered or computed)
- Substrate fabrication costs (entered, computed, or process flow)
- Surface mount and through-hole assembly costs
- Bare die attach costs (TAB, wirebond, flip chip)

- Tooling costs associated with assembly processes
- Test, repair, and rework costs

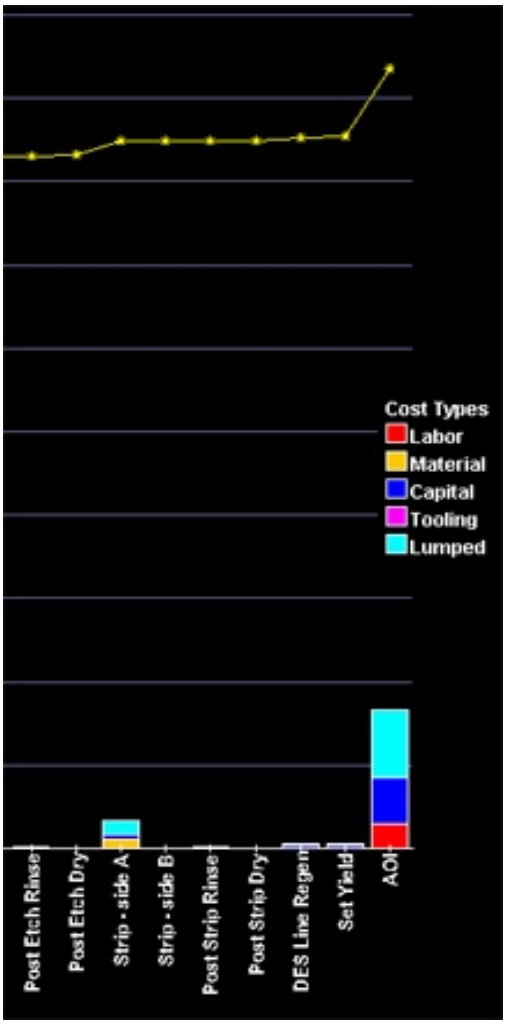

Figure 1 - Cost Plot

The plot in figure 1 shows the results of a *SavanSys* analysis.

The methodology for defining cost models in *SavanSys* is based on dividing the process into a series of activities and then defining the costs, times, and yields associated with each of those activities. Step types in *SavanSys* are one of the following.

- Substrate – This step calculates the cost and yield of the substrate using either a user defined calculation or running a substrate fabrication process flow.
- Component – This type of step adds the cost and yield of new components to a system.
- Assembly – This type of step is used to define board assembly activities.
- Processing – This type of step is used to define board fabrication activities.
- Test - This type of step defines testing activities. Defects introduced into the system by previous steps are detected by test steps and the board is either fixed through rework or scrapped.
- Rework – This type of step defines the repair or rework activities.

Figure 2 - Lamination Step Details

Step definitions in *SavanSys* vary slightly based on the type of step, but all steps include the follow basic information.

- Time – Used to calculate labor and equipment costs.
- Operator utilization and rate – Combined with time to get cost.
- Equipment utilization and cost – Combined with time and depreciation schedule to determine allocated cost.
- Defects in parts per million or defects per square cm – Used to calculate and accumulate the system yield.
- Tooling costs – Divided over the lifetime quantity of boards.

- Material and amount used – References the material data base to calculate material costs.

The screen shot in Figure 2 shows an example step definition for a lamination step.

Parameter Based vs. Activity Based Cost Modeling

Even though activity based cost modeling has a number of advantages over parameter based cost modeling, it also has some deficiencies. Table 1 below summarizes the pros and cons of both approaches.

Table 1 – Cost Modeling Comparison

	Simple Parameter Based Cost Modeling	**Activity Based Manufacturing Process Cost Modeling**
Accuracy	Poor - Simple models result in low accuracy	Good – Detailed process flows result in high accuracy
Initial Model Creation	Good – Easy to create a simple model in Excel	Poor – Manufacturing cost models must be built prior to doing tradeoffs
Ease of doing tradeoffs	Good – Quick and easy to modify a few parameters and re-run	Good – Easy to change technology or try different manufacturing models

The biggest drawback to cost modeling with activity based manufacturing models is the requirement to initially build the models. However, once these models are built, they can be used repeatedly for multiple new designs.

Simple, parameter based models are useful to understand whether or not embedding should be considered for a given design. If so, then more accurate modeling should be done to understand the exact costs and make the optimum technology selection.

Designs Suitable For Embedding

Based on the process models created in *SavanSys* and analyses done on a number of designs, following are general observations regarding design characteristics that warrant consideration for embedding. As noted previously, the specific costs vary greatly; therefore, the characteristics listed below should be used as a guide for consideration, not as a guide for ultimate decision making.

1. Designs with a significant percentage of passives compared to active components - Since a large portion of the extra fabrication costs associated with embedded passives are incurred on a per layer pair per panel basis and the costs associated with discrete passives are incurred on a per device basis, the economics improve if a large number of passives are embedded. Considering only the total number of embeddable passives in a design may be misleading because the extra fabrication cost is per panel, not per board. Therefore, a small board with a small number of embeddable passives still may be a good candidate because of the large number of boards per panel. The best metric for finding good candidate designs for embedding is to consider the number of embeddable passives relative to the total component count. These boards can often be shrunk with embedding

2. High performance designs - Designs with high performance requirements are excellent candidates for embedding because the maximum achievable operating frequency is greater with embedded passives than it is with discrete passives. In some cases, the electrical properties of the materials are superior, but the biggest performance advantage is due to a much shorter and simpler interconnect path between the high performance active devices and the embedded passives associated with those devices. Therefore, for high performance designs, the economic question associated with embedding is usually: “what is the optimal embedded design that achieves the performance requirements?”

3. Size constrained designs in which the limiting size factor is the board area required for components - Embedding passives should always be considered for designs with this characteristic. In some cases other options such as alternate component packaging, the use of daughter cards or sims, or alternate fabrication techniques will be a better choice than using embedded passives. However, in many cases embedding the passives will be the best option.

4. Designs which have excess routing capacity - The two significant cost adders for embedded passives board fabrication are extra costs associated with layer pairs which include embedded devices, and the cost of extra layer pairs. For designs that have a lot of excess routing capacity, it is likely that an embedded version of that design will have the same number of layer pairs. Designs containing high I/O count PGAs or BGAs often have significant excess routing capacity because a lot of interconnect layers are required to escape route the device, but those layers are not fully utilized in other regions of the board.

Design characteristics unsuitable for embedded passives

Designs that fit the characteristics below should not be considered.

1. Designs with a small percentage of passives relative to active components - It is unlikely that designs with a small percentage of embeddable passives per actives will be cheaper to embed since the design will probably not shrink and the density of embedded devices will probably be low.

2. Designs which are not size constrained or have a fixed board size - Designs that are not size (or performance) constrained can often be done cheaper with discretes. Component and assembly costs for 0402 discretes have fallen significantly over the past few years. In many cases the total cost is less than half a cent per placement, and unless the design has characteristics outlined in section a above, the discrete passives option is probably the cheapest option.

Conclusions / Future Trends

With continued market pressure for smaller, faster, and cheaper products, the economics of embedded passives will improve compared to discrete passives. As demonstrated by the IC manufacturing industry over the past forty years, as circuit devices become smaller they also become cheaper to fabricate. The opposite is true for mechanically placing very small objects (discrete passives). Therefore, it is not a matter of whether embedded passives will overtake discrete passives from a cost perspective, but rather exactly when.

Accurate cost modeling is crucial to know when that breakeven point occurs for every new design. Changing from discrete passives to embedded passives too soon will result in a product that costs more than it should and may be too expensive to succeed in its market. Changing over from discrete passives too late will have the same result, particularly if some of your competitors have made the change at the right time.

The only way to resolve this timing dilemma is to carefully and accurately analyze the specific design against the specific manufacturing target for that design.