Size and Cost Modeling for Embedded Passives

Chet Palesko
Leonard Roach
Answer Systems North America
www.answer-systems.com
Austin, Texas

Abstract
Lower cost is frequently listed as the main driver for moving to embedded passives. Unfortunately, understanding the true cost difference between a design using embedded passives and the same design using discrete passives is complicated. These discrepancies span design, board fabrication, materials, and assembly. While a variety of factors influence the cost difference, one of the major cost drivers involves layer count and board size. Designs with embedded passives often fit on smaller boards when compared to designs with discrete passives. However, although the cost per square inch of the embedded passives board is higher than the discrete alternative, the total cost of the smaller board may be less.

This paper analyzes drivers that influence the design size and layer count. A methodology is presented for accurately predicting the final size and cost of designs with embedded passives as well as with discrete passives. This methodology includes design routing analysis, escape routing analysis for BGA's, board surface area analysis, and panelization details. The cost impact of these size differences is also analyzed using activity based cost models for board fabrication and assembly.

Economic Drivers for Embedded Passives
The cost tradeoffs associated with the manufacture and assembly of boards containing embedded passives is complicated by differences in board fabrication and board assembly. This means the cost drivers associated with embedding passives are spread throughout the supply chain, making it extremely difficult to compare options.
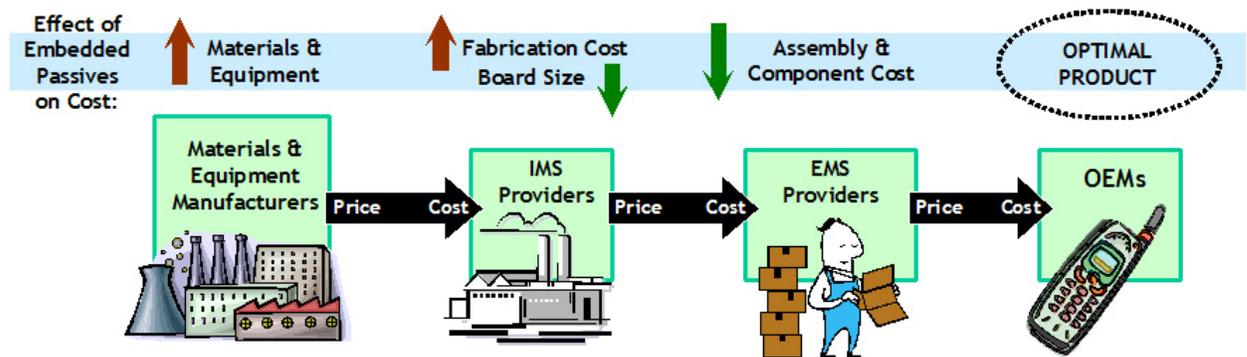

Figure 1 – Electronic Product Supply Chain

Figure 1 shows how the embedded passives cost is distributed across the supply chain. One of the main difficulties in determining the total cost is that variations in both cost and pricing must be considered. Even though the data is sometimes difficult to gather, cost can be measured and quantified. However, pricing may vary based on factors that have nothing to do with the actual cost. For example, large customers with tough purchasing departments will have better pricing for materials and boards compared to smaller companies. Therefore, similar designs may have very different costs due to diversity in the supply chain pricing.

Another challenge results from the fact that the actual cost of a material or process is often considered highly confidential. Because of this confidentiality, suppliers may publish an average price that they charge, and it will often be higher than the true average. (Nobody wants to publicize a price that is lower than what they charge any of their customers.) Using average published numbers makes it difficult to get an accurate model for a specific design.

In order to understand the difference between the cost of a board with embedded passives and the cost of the same board using discrete passives, it is helpful look at which costs are affected, and the rate at which they change. For example, adding two discrete capacitors to a design will cost twice as much as adding one discrete capacitor. However, the cost of two embedded capacitors on a board is the same as the cost of one embedded capacitor, because the cost of a capacitive layer pair is incurred on a per panel basis, not per device. The cost drivers for embedded passives can be grouped into the following three categories:

1. Increased board fabrication cost – The primary drivers that increase the board fabrication cost when embedding passives are increased material costs and the addition of extra processing steps. Most of the cost associated with the extra processing steps is incurred on a per panel basis. For example, the cost of adding a layer pair with a thin dielectric for embedded capacitors is the same whether there is one embedded capacitor on the panel or 10,000. However, some processing steps do have a substantial cost per device component as well as a cost per panel component. For example, the extra cost associated with laser trimming resistors contains a small cost that is independent of the number of resistors to be trimmed, as well as a larger cost that is dependent on the number of resistors trimmed. The location and the layout of the design also have a large influence on the cost per trimmed resistor. The net result is that these costs are heavily design dependent.

While most of the extra processing costs are driven on a per panel basis, some of the extra material costs are driven on a per device and per panel basis. As noted above, the extra material cost for an embedded capacitance layer pair is purely per panel. However, the material cost for ceramic devices and the ink for printed devices vary based on the number of devices.

2. Decreased board assembly and component cost – Since the embedded devices replace discrete devices, the cost of assembling the board is reduced. The direct cost improvements include the cost of the replaced components plus the cost of placing those components on the board. Additionally, a board with embedded devices will have higher yield and reliability due to fewer solder joints. A significant reduction in the board assembly cost may be achieved for boards that can be converted from two sides to a single side.

3. Decreased board size/cost – In many cases, the surface real estate for placing components is the limiting factor on board size. In these designs, the use of embedded passives may result in a smaller board. If the size reduction is enough to yield more boards per panel, the board fabrication cost of the embedded design may be less than the non-embedded option even though the cost per square inch of embedding is higher.

Board Size and Layer Count
The reduction in board size enabled by the use of embedded passives is often the dominant factor that influences the cost of the design. Unfortunately, because the size difference between a design with embedded passives compared to a design with discrete passives may be difficult to determine, it is often ignored, and the result is a sub-optimal design.

Any of the following factors may influence board size and layer count. However, it is important to note that each design will be dominated by one factor that drives the minimum board size (area and layer count). For example, even if a design has sparse routing requirements, a single high pin count BGA may drive the minimum number of layers on a board due to escape routing needs.

1. Board surface area required to place all the components – The surface area of a board is often the size limiting factor. For each component in the design, enough area must be available to place the component (including required manufacturing spacing) and to connect to the component. Designers can trade off surface area for layer count by choosing the appropriate package. Chip scale packaging minimizes the surface area, but the bond pad density may drive the layer count higher. On the other hand, larger packages take up more area, but require fewer layers for escape routing.

2. Routing area needed to connect all the components – In addition to area requirements driven by each component, a board must have enough routing area to connect the components. This usually drives the number of layers in the design. While the exact percentage of resources needed compared to resources available varies by design style and CAD system, a design that uses less than or equal to 50% of the available area can often be automatically routed.

3. System level constraints that fix one or more of the board dimensions – System level constraints such as connectors to a backplane or physical package limits will often dictate the maximum and minimum board dimensions. To stay within the maximum board size, chip scale packaging and double sided layout are often used.

As noted above, compromises made to decrease the size of the board usually force the addition of more layers. Alternately, if the board has a minimum size constraint, packaging decisions should be made to reduce the layer count and, if possible, to use only one side of the board.

4. Electrical or thermal constraints – The size of high speed, analog, RF, and analog mixed signal boards is often driven by performance requirement, not by component and routing density. Special routing, shielding, additional ground, planes, etc. found in these designs may increase the size of the board and its layer count. In addition, thermal management drives boards to be larger as well.

5. Escape routing for BGAs – As noted above, escape routing requirements for high density BGAs may drive the layer count to be higher than what is necessary to accommodate the overall design routing requirements.

The use of embedded passives is another tool which designers can use to manage the board sizing. Discrete passives consume surface area which, in many designs, is the limiting factor on size. Converting these discrete passives to embedded passives frees up surface area and instead consumes routing resource on one or more internal layers. This tradeoff is similar to the chip scale package tradeoff, and in size critical designs, both chip scale packages and embedded passives should be considered.

SavanSys **Overview**
Below is a brief description of the *SavanSys* activity based cost modeling technology. For additional information on the capabilities and availability of this technology, please contact the authors.

SavanSys is a cost modeling and technology tradeoff tool. Data is extracted from the design tool environment to create a physical representation of the design. Activity based models of both board fabrication and assembly are created to model the manufacturing process. This combination of design and manufacturing information is used to generate a "virtual prototype" of the board to accurately determine size, cost, and yield. The results of this model are extremely accurate because it considers the details of the target board applied to a specific manufacturing environment with precise costs and yields.

The data considered by *SavanSys* for doing this analysis is listed below.

The Design Model in SavanSys
Because of the substantial number of packaging technologies, processes, and materials that are available, making optimum choices is not a trivial task. Alternative technologies and materials include:
* Substrates (printed circuit boards, ceramic, thin-film, etc.)
* Chip packaging
* Bonding techniques (wirebond, TAB, flip chip)
* Test techniques
* Manufacturing methods

SavanSys accepts physical information that describes multiple chips (or bare die) and their interconnection. All of the information that is collected by *SavanSys* is physical, as opposed to logical, behavioral, or functional. *SavanSys* does not import VHDL or similar behavioral information because such descriptions do not contain a significant amount of useful physical information. *SavanSys* accepts the following physical inputs.

Chips (bare die and packaged die):
* Dimensions (length, width, thickness)
* I/O type and count
* Cost and yield

Chip Packaging:
* Bonding (technology, materials, and design rules)
* Encapsulation (materials and design rules)
* Die attach (materials and design rules)
* Process flow information (chip preparation, testing, and burn-in)

Boards/Modules:
* Substrate (technology, materials, and design rules)

- Connectorization (technology, materials, and design rules)
- Process flow information (substrate fabrication)

In *SavanSys*, netlists are optional because tradeoff activities often take place prior to the presence of a detailed netlist. Therefore, the total number of nets in a partition can be estimated with *SavanSys* even without a detailed netlist.

Module size prediction is accomplished by computing the following set of footprints for each component (active and passive) in the board.
- The interconnect-capacity footprint is the size limitation based on the amount of wiring required to connect a component within the module. It depends on the wiring capacity of the substrate and the quality of the routing.
- The via-density footprint accounts for the number of vias that are available to connect component I/O to wiring layers.
- The bond-pad-density footprint accounts for the distribution of bond pads on the surface of the interconnecting substrate.
- The escape-routing footprint analyzes routing component I/O out from under the die, either to wiring tracks on the surface of substrates or to vias that connect to other wiring layers.
- The placement or die footprint represents the physical size of the bare die or packaged chip and its surrounding bonds, as well as minimum spacing to adjacent components.

In order to obtain the module area, the footprints representing each component are appropriately accumulated.

The Manufacturing Model in SavanSys
SavanSys cost models may include the following costs. Given that the costs below are optional, *SavanSys* models can be used to analyze total system costs or specific components of the system cost.
- Component costs (entered or computed)
- Component preparation (process may be defined)
- Single chip package costs (entered or computed)
- Substrate fabrication costs (entered, computed, or process flow)
- Surface mount and through-hole assembly costs
- Bare die attach costs (TAB, wirebond, flip chip)
- Tooling costs associated with assembly processes
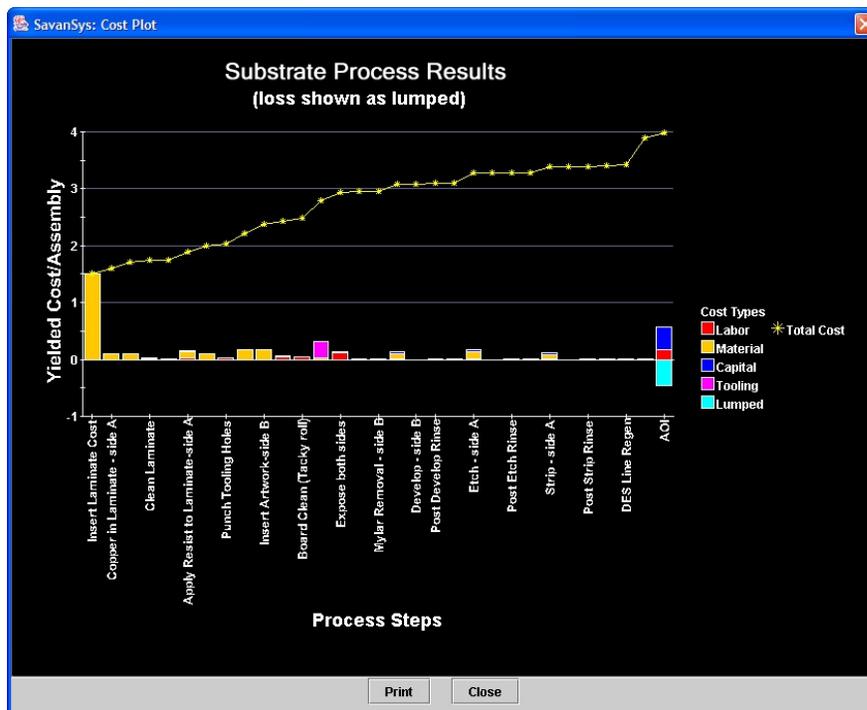- Test, repair, and rework costs

Figure 2 - Cost Plot

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The plot in Figure 2 shows the results of a *SavanSys* analysis.

The methodology for defining cost models in *SavanSys* is based on dividing the process into a series of activities and then defining the costs, times, and yields associated with each of those activities. Step types in *SavanSys* are one of the following.
- Substrate – This step calculates the cost and yield of the substrate using either a user defined calculation or running a substrate fabrication process flow.
- Component – This type of step adds the cost and yield of new components to a system.
- Assembly – This type of step is used to define board assembly activities.
- Processing – This type of step is used to define board fabrication activities.
- Test - This type of step defines testing activities. Defects introduced into the system by previous steps are detected by test steps, and the board is either fixed through rework or scrapped.
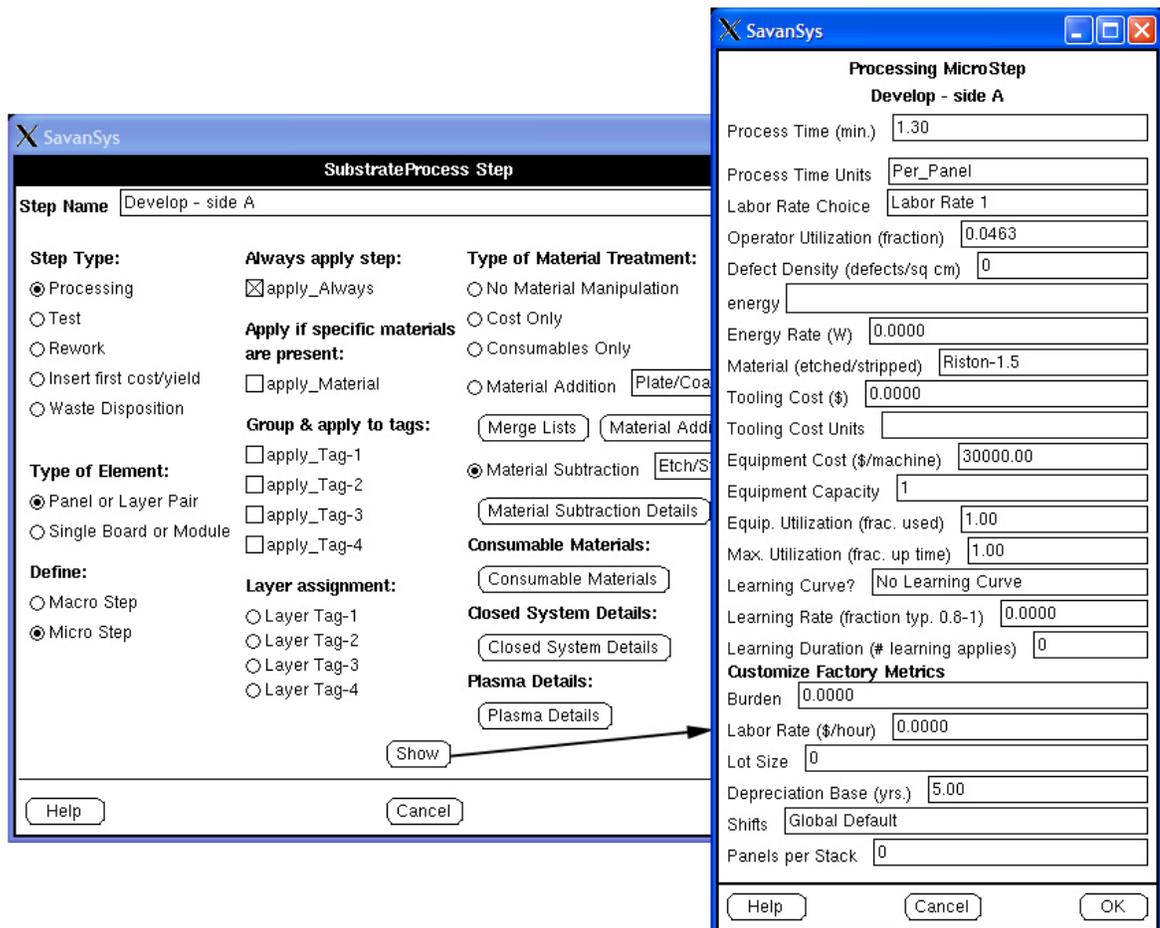- Rework – This type of step defines the repair or rework activities.

Figure 3 – Develop Step Details

Step definitions in *SavanSys* vary slightly based on the type of step, but all steps include the follow basic information.
- Time – Used to calculate labor and equipment costs.
- Operator utilization and rate – Combined with time to get cost.
- Equipment utilization and cost – Combined with time and depreciation schedule to determine allocated cost.
- Defects in parts per million or defects per square cm – Used to calculate and accumulate the system yield.
- Tooling costs – Divided over the lifetime quantity of boards.
- Material and amount used – References the material database to calculate material costs.

The screen shot in Figure 3 shows an example step definition for a develop step.

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Example Design – Trade Off Methodology

To illustrate an embedded passives trade off analysis, the SavanSys technology described above was used on an example design. The methodology for this design trade off is described below.

1. Determine the minimum board size and layer count using discrete passives. – Since the size (area and layers) directly drives the cost of the board, the size must be determined before looking at any other factors. For this example, we determined the minimum board size by doing an initial placement of the components and measuring the packing density. The packing density is the total component area divided by the surface area of the board. The maximum density achievable was 44.59%. The minimum layer count was six layers; although the total routing utilization was only 17.34%, this value was driven by the escape routing needed for a 680 pin BGA. Figure 4 displays these size results.

Figure 4 – Baseline Size Results of the Example Design

2. Determine the total cost of this design. – The next step was to calculate the total cost of the design including substrate cost, assembly cost, and component cost.

3. Embed selected passives. – The next step was to select which devices to embed. In this example, we selected resistors and capacitors and embedded them using a ceramic paste process. A total of 541 capacitors ranging in value from 1,000PF to .1UF and 993 resistors ranging in value from 100 ohms to 1K ohms were embedded.

4. Determine the minimum board size and layer count with embedded passives. – To determine the minimum board size using embedded passives, we set the packing density from the baseline version as a maximum, and we shrunk the board until that value was reached. We then analyzed the total area required to embed the devices and determined that all the selected devices would fit on 2 layers. However, the area on the layers taken up by the devices was no longer available for signal routing. Therefore, the routing utilization climbed and was analyzed to determine if additional layers were required. For this design, no additional layers were necessary.

5. Determine the cost of the embedded design and compare the results – The final step was to calculate the cost of the embedded version of the design and compare this to the discrete version. Because all manufacturing costs (components, board fabrication, and board assembly) were included, the smallest total cost was the cheapest alternative.

Example Design - Results
The table below illustrates the results of this design.

	Baseline	**Embedded - No Size Reduction**	**Embedded with Size Reduction**
Board Size	93.6 sq. in.	93.6 sq. in.	86.9 sq.in.
Layer count	6	6 (2 embedded)	6 (2 embedded)
Number Up on Panel	2	2	4
Packing Density	44.59%	41.38%	44.57%
Routing Utilization	17.34%	26.62%	27.79%
First Pass Yield (at ICT)	77%	88%	88%
Assembly Cost	$47.99	$40.09	$40.09
Component Cost	$228.77	$222.50	$222.50
Substrate Cost	$88.54	$103.28	$60.91
TOTAL COST	**$365.30**	**$365.87**	**$323.50**

Table 1 – Embedded vs. Discrete Passives for the Example Design

The lowest cost option for this design was the embedded version with a board size reduction shown in the third column. The discrete version of this design was limited by the surface area, but had excess routing resources in the board. Packing density was an important metric, because we were able to use it to compare design alternatives while holding the density equal. A design with high packing density and low routing utilization is an excellent candidate for embedded passives.

Another indication that this design could benefit from embedding was the low first pass yield during assembly. A significant factor that caused this low yield was the large number of discretes to be placed. Improving this first pass yield significantly lowered the test and rework costs during board assembly.

The board area of the embedded option was reduced by 7%. However, the number of boards up on a panel went from two to four, which resulted in a cost reduction much greater than 7%. This situation highlighted the importance of considering the panelization issues for the board, instead of taking into account only the pure size reduction. Considering panelization is particularly critical for large boards since small changes in size may yield large changes in cost. Another significant issue which contributed to the cost saving was the 11% increase in the first pass yield, which saved almost $8.00 in assembly cost.

A third option is included in the table (column 2) to highlight why board size is a vital factor for the embedded passives decision. If size had been ignored in this design, the discrete version would have been less expensive than the embedded version, as can be seen in columns one and two. This displays that only using discrete passives would have been a suboptimal decision for this design.

Summary and Conclusions
With continued market pressure for smaller, faster, and cheaper products, the economics of embedded passives will improve compared to discrete passives. As demonstrated by the IC manufacturing industry over the past forty years, as circuit devices become smaller, they also become cheaper to fabricate. The opposite is true for mechanically placing very small objects (discrete passives). Therefore, it is not a matter of whether embedded passives will overtake discrete passives from a cost perspective, but rather exactly when.

Accurate cost modeling is crucial to know when that breakeven point occurs for every new design. To achieve this accurate cost analysis, attention must be paid to all the cost drivers. In particular, accurate size analysis must include escape routing, total routing, packing density, and panelization details. Without considering all of these factors, designers will miss opportunities to save money with embedded passives.

The only way to resolve this timing dilemma is to carefully and accurately analyze the specific design against the specific manufacturing target for that design.